



National Semiconductor

June 1996

# 54AC/74AC245 • 54ACT/74ACT245 Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

TL/F/9944-2

## 54AC/74AC245 • 54ACT/74ACT245 Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

### General Description

The 'AC/'ACT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

### Features

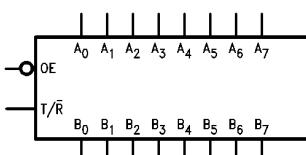
- I<sub>CC</sub> and I<sub>OZ</sub> reduced by 50%
- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA
- 'ACT245 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC245: 5962-87758
  - 'ACT245: 5962-87663

Commercial	Military	Package Number	Package Description
74ACT245PC		N20A	20-Lead Molded Dual-In-Line (0.300" Wide)
74ACT245SC (Note 1)		M20B	20-Lead Molded Small Outline (0.300" Wide), JEDEC
74ACT245SJ (Note 1)		M20D	20-Lead Molded Small Outline, EIAJ Type II
74ACT245MTC (Note 1)		MTC20	20-Lead Molded Thin Shrink Small Outline Package, JEDEC
74ACT245MSA (Note 1)		MSA20	20-Lead Molded Small Shrink Outline Package, (EIAJ SSOP)
	54ACT245DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
	54ACT245FM (Note 2)	W20A	20-Lead Cerpak
	54ACT245LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" Tape and Reel. Use suffix SCX, SJX, and MTCX.

Note 2: Military grade device with environmental and burn-in processing, use suffix DMQB, FMQB and LMQB.

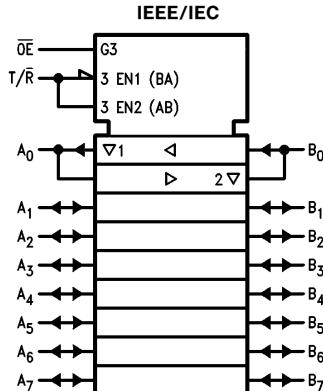
### Logic Symbols



TL/F/9944-1

Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A <sub>0</sub> -A <sub>7</sub>	Side A TRI-STATE Inputs or TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Side B TRI-STATE Inputs or TRI-STATE Outputs

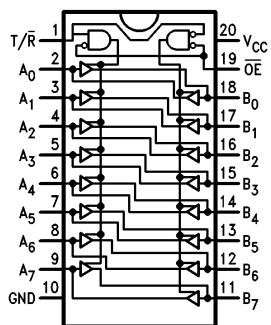
TRI-STATE® is a registered trademark of National Semiconductor Corporation.  
FACT™ is a trademark of National Semiconductor Corporation.



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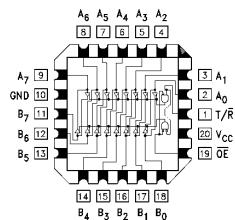
## Connection Diagrams

**Pin Assignment for DIP,  
Flatpak, SSOP, SOIC and TSSOP**



TL/F/9944-3

**Pin Assignment for LCC**



TL/F/9944-4

## Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	$-0.5V$ to $+7.0V$
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	$-20\text{ mA}$
$V_I = V_{CC} + 0.5V$	$+20\text{ mA}$
DC Input Voltage ( $V_I$ )	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	$-20\text{ mA}$
$V_O = V_{CC} + 0.5V$	$+20\text{ mA}$
DC Output Voltage ( $V_O$ )	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50\text{ mA}$
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50\text{ mA}$
Storage Temperature ( $T_{STG}$ )	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Junction Temperature ( $T_J$ )	
CDIP	$175^{\circ}\text{C}$
PDIP	$140^{\circ}\text{C}$

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	$2.0V$ to $6.0V$
'AC	$4.5V$ to $5.5V$
'ACT	
Input Voltage ( $V_I$ )	$0V$ to $V_{CC}$
Output Voltage ( $V_O$ )	$0V$ to $V_{CC}$
Operating Temperature ( $T_A$ )	
$74AC/ACT$	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
$54AC/ACT$	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'AC Devices	
$V_{IN}$ from $30\%$ to $70\%$ of $V_{CC}$	
$V_{CC}$ @ $3.3V$ , $4.5V$ , $5.5V$	$125\text{ mV/ns}$
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from $0.8V$ to $2.0V$	
$V_{CC}$ @ $4.5V$ , $5.5V$	$125\text{ mV/ns}$

## DC Characteristics for 'AC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	74AC		54AC	74AC	Units	Conditions
			$T_A = +25^{\circ}\text{C}$		$T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	2.1 3.15 3.85	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
$V_{IL}$	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	0.9 1.35 1.65	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
$V_{OH}$	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	2.9 4.4 5.4	V	$I_{OUT} = -50\text{ }\mu\text{A}$
		3.0 4.5 5.5		2.56 3.86 4.86	2.4 3.7 4.7	2.46 3.76 4.76	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $-12\text{ mA}$ $I_{OH} = 24\text{ mA}$ $-24\text{ mA}$
$V_{OL}$	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V	$I_{OUT} = 50\text{ }\mu\text{A}$
		3.0 4.5 5.5		0.36 0.36 0.36	0.50 0.50 0.50	0.44 0.44 0.44	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $12\text{ mA}$ $I_{OL} = 24\text{ mA}$ $24\text{ mA}$
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	$V_I = V_{CC}, \text{ GND}$

\*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74AC		54AC	74AC	Units	Conditions	
			T <sub>A</sub> = + 25°C		T <sub>A</sub> = - 55°C to + 125°C	T <sub>A</sub> = - 40°C to + 85°C			
			Typ	Guaranteed Limits					
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5		50	75	mA	V <sub>OLD</sub> = 1.65V Max		
I <sub>OHD</sub>		5.5		-50	-75	mA	V <sub>OHD</sub> = 3.85V Min		
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	4.0	80.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND		
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5	±0.3	±6.0	±3.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND		

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74ACT		54ACT	74ACT	Units	Conditions
			T <sub>A</sub> = + 25°C		T <sub>A</sub> = - 55°C to + 125°C	T <sub>A</sub> = - 40°C to + 85°C		
			Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	2.0	2.0	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	1.5	0.8	0.8	0.8		
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.49	5.4	5.4	5.4		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	3.86	3.70	3.76	3.76	V	*V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA
		5.5	4.86	4.70	4.76	4.76		I <sub>OH</sub> = -24 mA
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±0.1	±1.0	±1.0	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
		5.5	0.001	0.1	0.1	0.1		
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.6	1.5	mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		5.5						
I <sub>OLD</sub>	†Minimum Dynamic Output Current	5.5		50	75	mA	V <sub>OLD</sub> = 1.65V Max	
		5.5		-50	-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	4.0	80.0	40.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND	
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5	±0.3	±6.0	±3.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND	

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

### AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			54AC		74AC		Units	
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.5	1.0 1.0	11.5 8.5	1.0 1.0	9.0 7.0	ns	
t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	3.3 5.0	1.5 1.5	5.0 3.5	8.5 6.0	1.0 1.0	10.0 7.5	1.0 1.0	9.0 7.0	ns	
t <sub>PZH</sub>	Output Enable Time	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	1.0 1.0	13.5 10.0	2.0 1.0	12.5 9.0	ns	
t <sub>PZL</sub>	Output Enable Time	3.3 5.0	2.5 1.5	7.5 5.5	12.0 9.0	1.0 1.0	14.5 10.5	2.0 1.0	13.5 9.5	ns	
t <sub>PHZ</sub>	Output Disable Time	3.3 5.0	2.0 1.5	6.5 5.5	12.0 9.0	1.0 1.0	13.5 10.5	1.0 1.0	12.5 10.0	ns	
t <sub>PLZ</sub>	Output Disable Time	3.3 5.0	2.0 1.5	7.0 5.5	11.5 9.0	1.0 1.0	14.0 10.5	1.5 1.0	13.0 10.0	ns	

\*Voltage Range 3.3 is 3.3V ± 0.3V  
Voltage Range 5.0 is 5.0V ± 0.5V

### AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			54ACT		74ACT		Units	
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	4.0	7.5	1.0	9.0	1.5	8.0	ns	
t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	5.0	1.5	4.0	8.0	1.0	10.0	1.0	9.0	ns	
t <sub>PZH</sub>	Output Enable Time	5.0	1.5	5.0	10.0	1.0	12.0	1.5	11.0	ns	
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	5.5	10.0	1.0	13.0	1.5	12.0	ns	
t <sub>PHZ</sub>	Output Disable Time	5.0	1.5	5.5	10.0	1.0	12.0	1.0	11.0	ns	
t <sub>PLZ</sub>	Output Disable Time	5.0	2.0	5.0	10.0	1.0	12.0	1.5	11.0	ns	

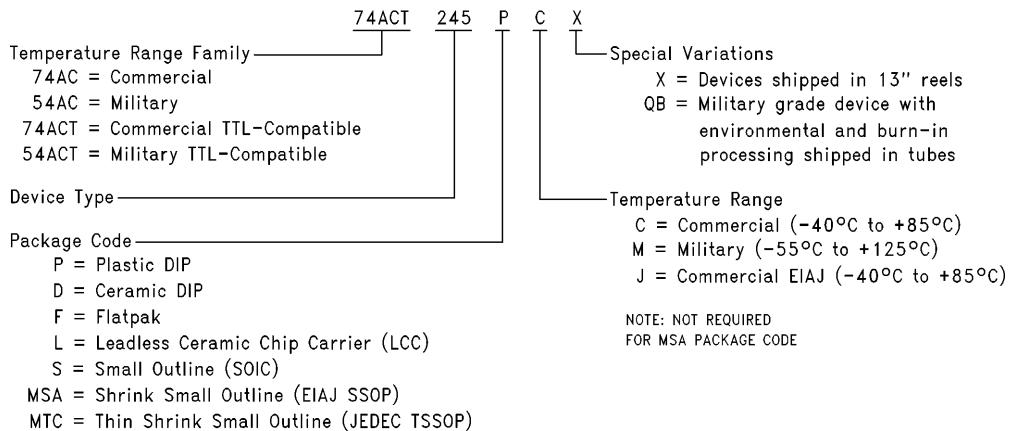
\*Voltage Range 5.0 is 5.0V ± 0.5V

### Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>I/O</sub>	Input/Output Capacitance	15.0	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	45.0	pF	V <sub>CC</sub> = 5.0V

## Ordering Information

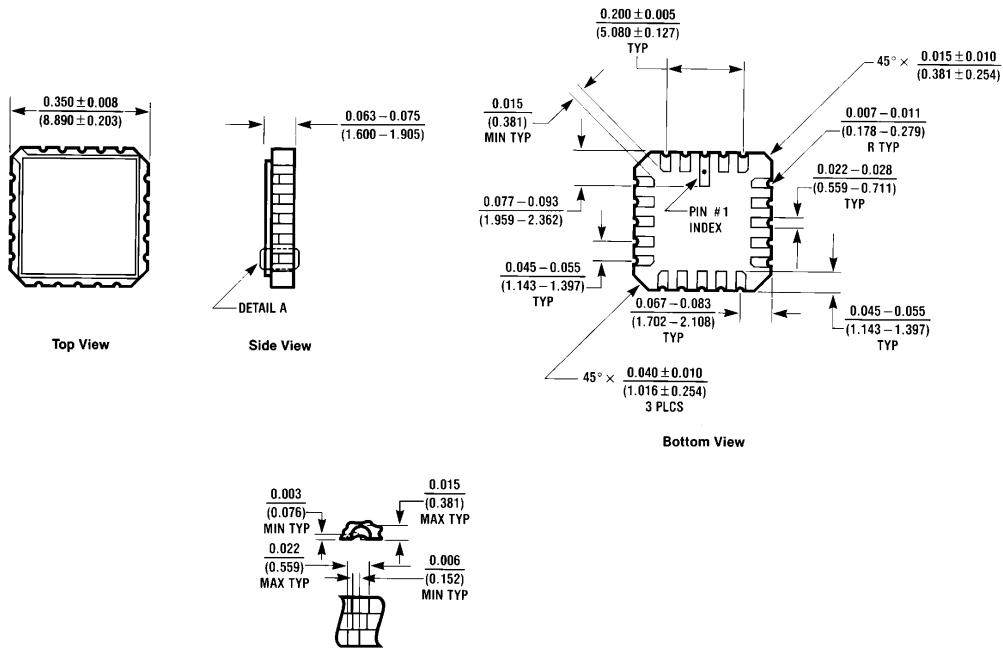
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



TL/F/9944-6

## Physical Dimensions

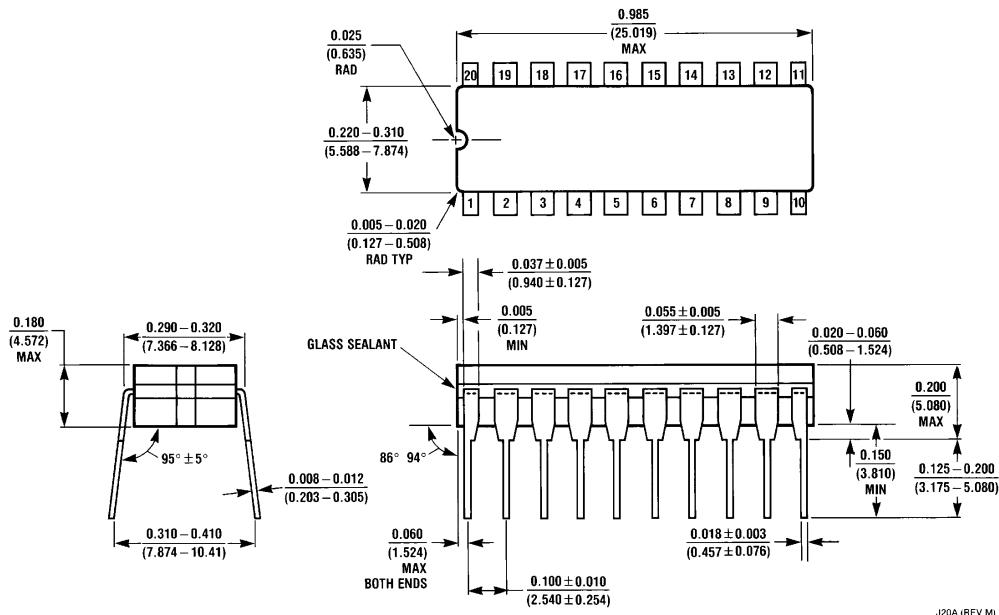
inches (millimeters) unless otherwise noted



20 Terminal Ceramic Leadless Chip Carrier (L)  
 NS Package Number E20A

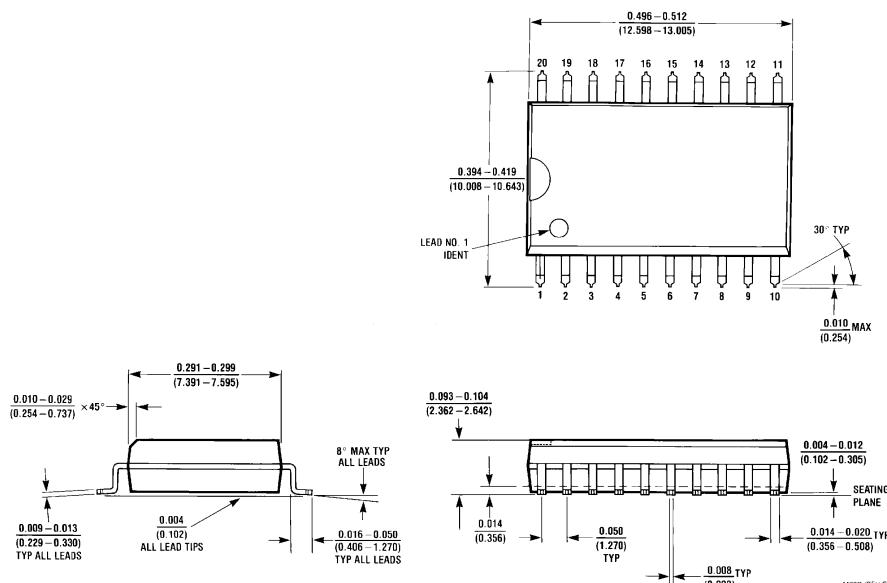
E20A (REV D)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



J20A (REV M)

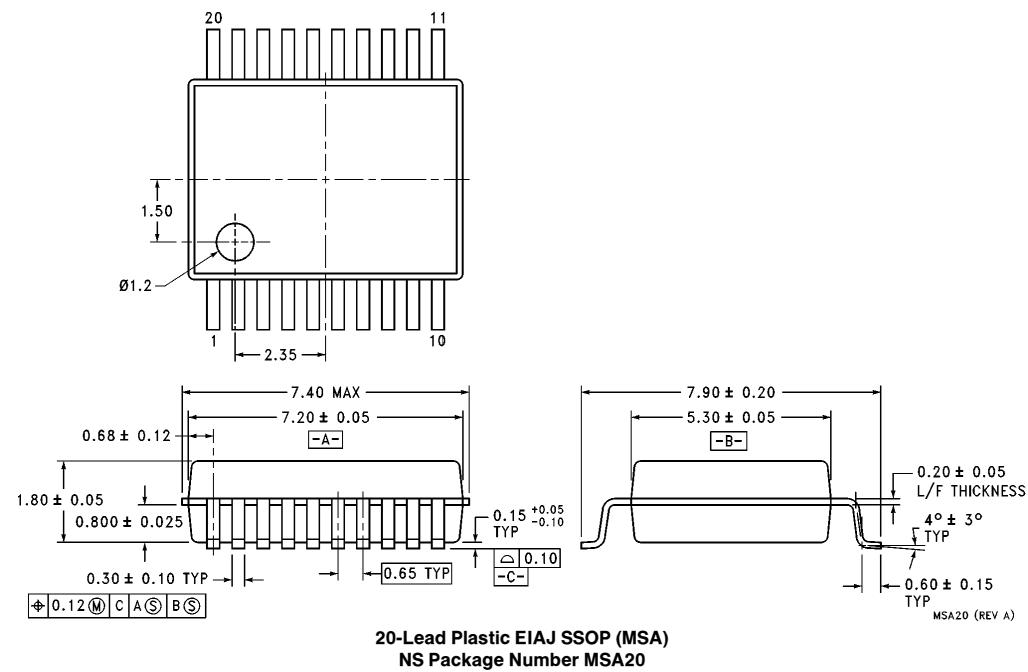
20-Lead Ceramic Dual-In-Line Package (D)  
NS Package Number J20A



M20B (REV F)

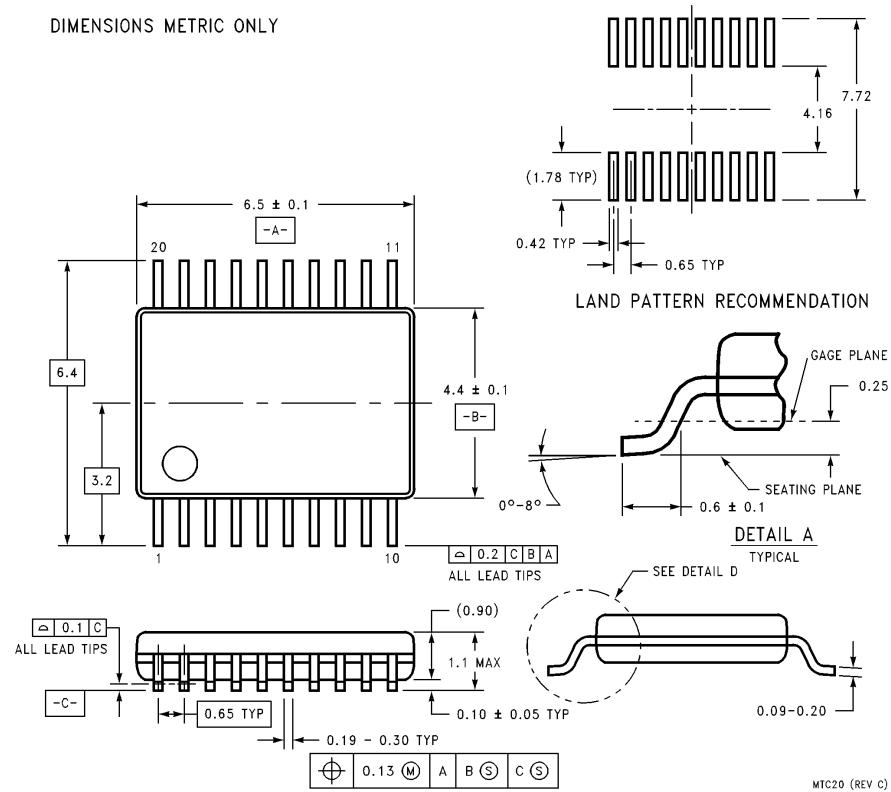
20-Lead Small Outline Integrated Circuit (S)  
NS Package Number M20B

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

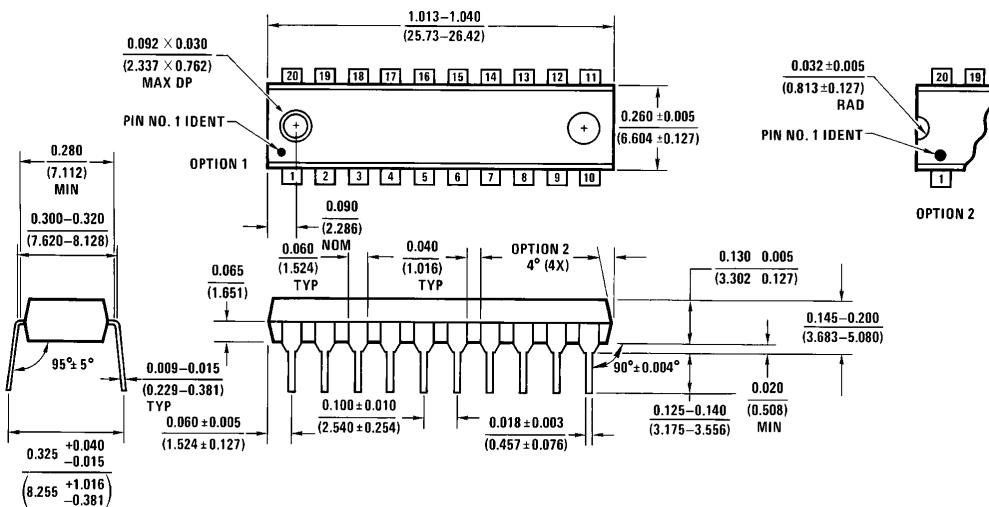


## **Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

**DIMENSIONS METRIC ONLY**



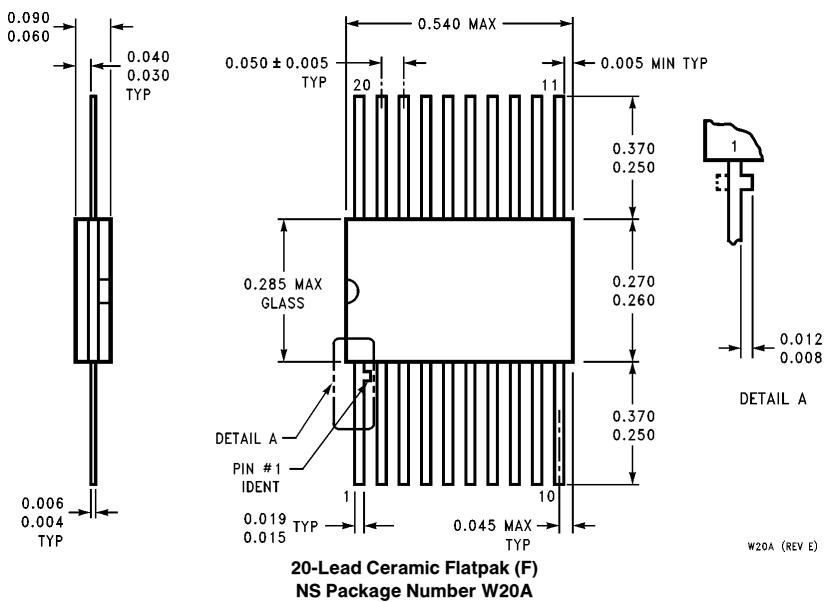
**20-Lead Molded Thin Shrink Small Outline Package, JEDEC  
NS Package Number MTC20**



**20-Lead Plastic Dual-In-Line Package (P)  
NS Package Number N20A**

**54AC/74AC245 • 54ACT/74ACT245**  
**Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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54ACT245 - <http://www.ti.com/product/54act245?HQS=TI-null-null-dscatalog-df-pf-null-wwe>

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