CMOS DUAL 4-BIT LATCH

FEATURES

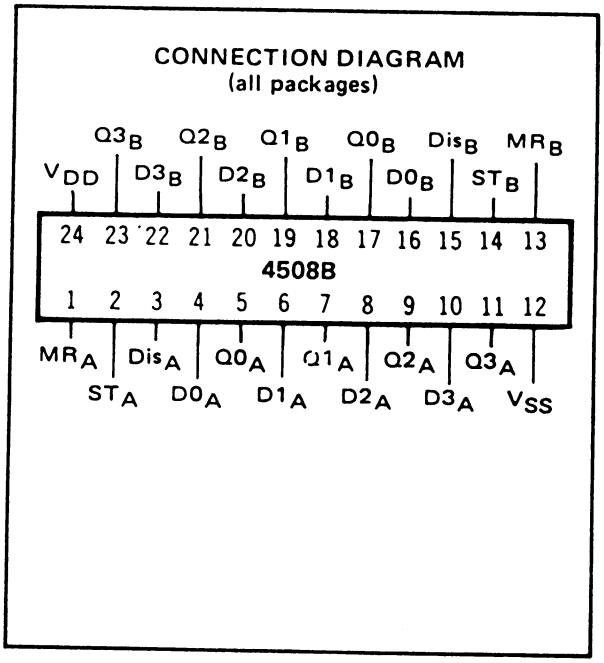
- Two Independent Four-Bit Latches
- 3-State Outputs
- Direct Reset
- All Inputs Buffered

DESCRIPTION

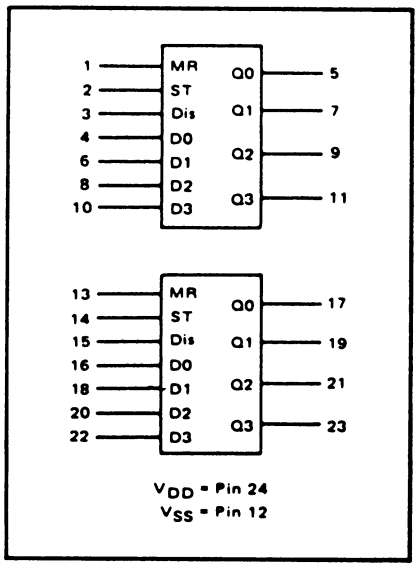
The 4508B consists of two identical independent 4-Bit Latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high-impedance state for bus line applications.

These devices find primary use in buffer storage, holding register, and display circuits, and other general digital logic applications.

CONNECTION DIAGRAM
(all packages)



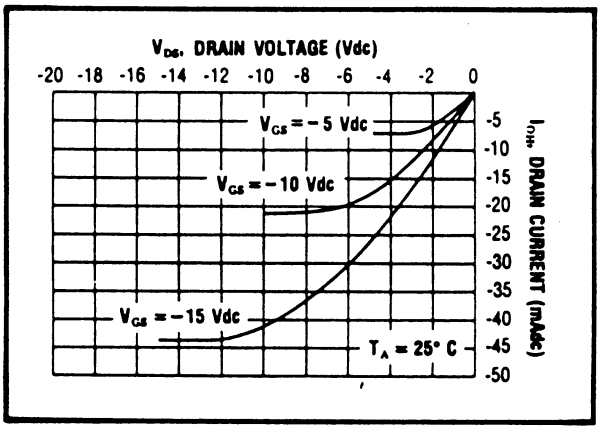
BLOCK DIAGRAM



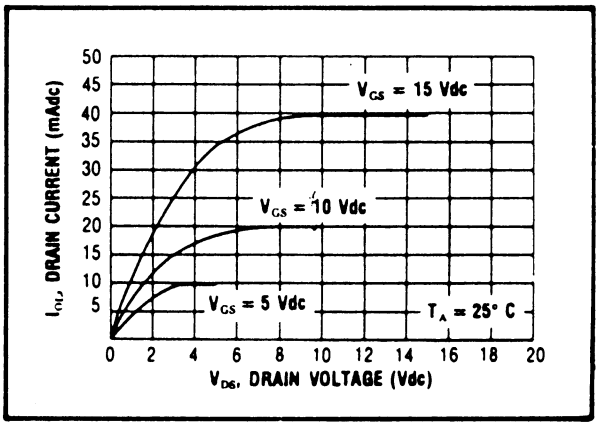
TRUTH TABLE

MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

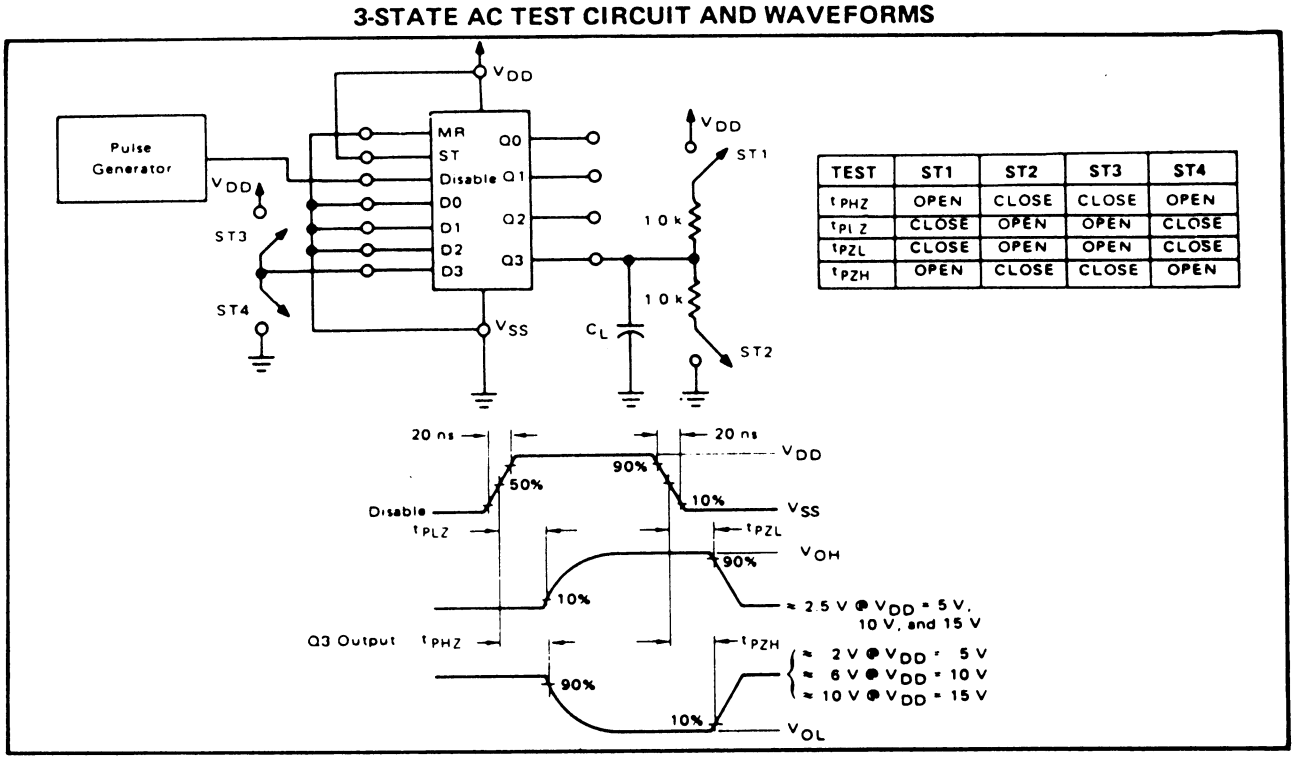
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW}		+25°C			T_{HIGH}		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm 10^{-4}$	±0.1	–	±1.0	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME						
From Data Inputs	t_{PLH}, t_{PHL}	5	–	220	440	ns
		10	–	90	180	
		15	–	60	120	
From Disable Input	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5	–	85	170	ns
		10	–	45	90	
		15	–	30	60	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM MASTER RESET PULSE WIDTH	PW_{MR}	5	–	100	200	ns
		10	–	50	100	
		15	–	35	70	
MINIMUM STROBE PULSE WIDTH	PW_{ST}	5	–	70	140	ns
		10	–	35	70	
		15	–	20	40	
MINIMUM SETUP TIME Data Inputs	t_{setup}	5	–	25	50	ns
		10	–	10	20	
		15	–	5	10	
MINIMUM HOLD TIME Data Inputs	t_{hold}	5	–	0	0	ns
		10	–	0	0	
		15	–	0	0	

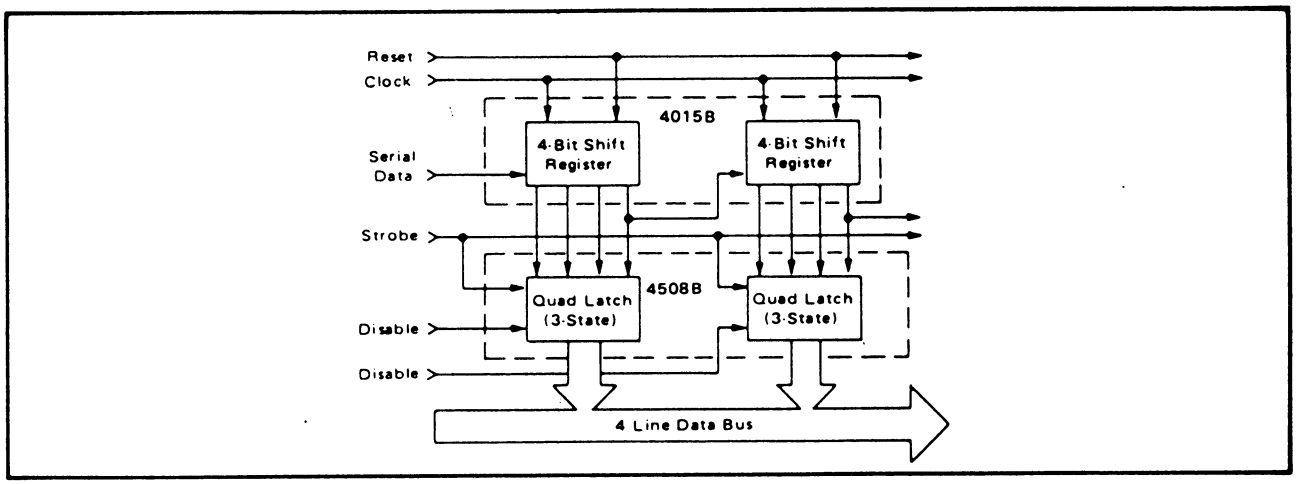
3-STATE AC TEST CIRCUIT AND WAVEFORMS



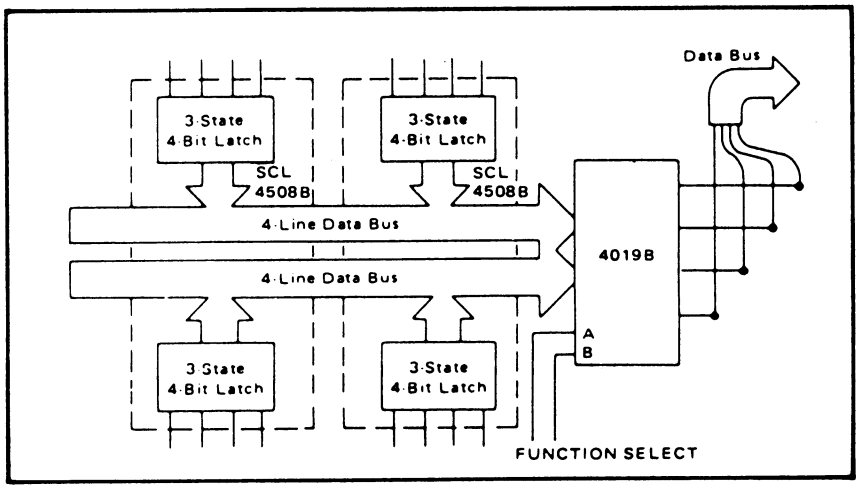
TEST	ST1	ST2	ST3	ST4
t_{PHZ}	OPEN	CLOSE	CLOSE	OPEN
t_{PLZ}	CLOSE	OPEN	OPEN	CLOSE
t_{PZL}	CLOSE	OPEN	OPEN	CLOSE
t_{PZH}	OPEN	CLOSE	CLOSE	OPEN

APPLICATIONS INFORMATION

BUS REGISTER



DUAL MULTIPLEXED BUS REGISTER WITH FUNCTION SELECT



FUNCTION SELECT

A	B	Function
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_i + B_i$