

**MC14501UB**

**Triple Gate**  
**Dual 4-Input "NAND" Gate**  
**2-Input "NOR/OR" Gate**  
**8-Input "AND/NAND" Gate**

The MC14501UB is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

**MAXIMUM RATINGS\*** (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

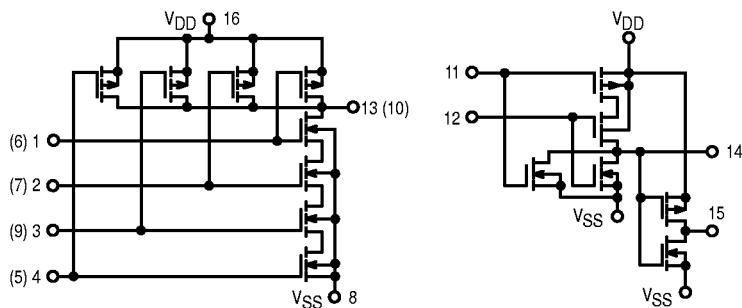
\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

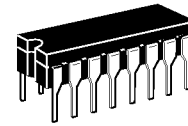
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

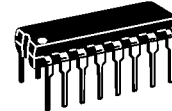
**CIRCUIT SCHEMATIC**



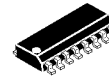
Numbers in parenthesis are for second 4-input gate.



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



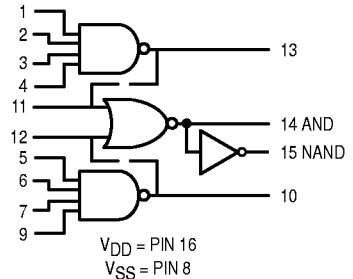
**D SUFFIX**  
SOIC  
CASE 751B

**ORDERING INFORMATION**

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBD SOIC

T<sub>A</sub> = - 55° to 125°C for all packages.

**LOGIC DIAGRAM**  
(POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

NOTE: Pin 14 must not be used as an input to the inverter.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to  $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level ( $V_O = 3.6$ or $1.4$ Vdc) ( $V_O = 7.2$ or $2.8$ Vdc) ( $V_O = 11.5$ or $3.5$ Vdc)  "1" Level ( $V_O = 1.4$ or $3.6$ Vdc) ( $V_O = 2.8$ or $7.2$ Vdc) ( $V_O = 3.5$ or $11.5$ Vdc)	$V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.4	Vdc	
		10	—	3.0	—	4.50	3.0	—	2.9		
		15	—	3.75	—	6.75	3.75	—	3.6		
	$V_{IH}$	5.0	3.6	—	3.5	2.75	—	3.5	—		Vdc
		10	7.1	—	7.0	5.50	—	7.0	—		
		15	11.4	—	11.25	8.25	—	11	—		
Output Drive Current ( $V_{OH} = 2.5$ Vdc) Source ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) NAND* ( $V_{OH} = 13.5$ Vdc)  ( $V_{OH} = 2.5$ Vdc) NOR ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  ( $V_{OH} = 2.5$ Vdc) NOR– ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) Inverter ( $V_{OH} = 13.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) Sink ( $V_{OL} = 0.5$ Vdc) NAND* ( $V_{OL} = 1.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) NOR ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)  ( $V_{OL} = 0.4$ Vdc) NOR– ( $V_{OL} = 0.5$ Vdc) Inverter ( $V_{OL} = 1.5$ Vdc)	$I_{OH}$	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc	
		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—		
		10	-0.62	—	-0.5	-0.9	—	-0.35	—		
		15	-1.8	—	-1.5	-3.5	—	-1.1	—		
		5.0	-2.1	—	-1.75	-3.0	—	-1.22	—		mAdc
		5.0	-0.42	—	-0.35	-0.63	—	-0.24	—		
	10	-1.06	—	-0.88	-1.58	—	-0.62	—			
	15	-3.1	—	-2.63	-6.12	—	-1.84	—			
	5.0	-3.6	—	-3.0	-5.1	—	-2.1	—	mAdc		
	5.0	-0.72	—	-0.6	-1.08	—	-0.42	—			
	10	-1.8	—	-1.5	-2.7	—	-1.05	—	mAdc		
	15	-5.4	—	-4.5	-10.5	—	-3.15	—			
	$I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc	
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
		5.0	0.92	—	0.77	1.32	—	0.54	—	mAdc	
		10	2.34	—	1.95	3.37	—	1.36	—		
		15	6.12	—	5.1	13.2	—	3.57	—		
5.0	1.54	—	1.28	2.2	—	0.90	—	mAdc			
10	3.90	—	3.25	5.63	—	2.27	—				
15	10.2	—	8.5	22	—	5.95	—				
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc	
Input Capacitance ( $V_{in} = 0$ )	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	0.25	—	0.0005	0.25	—	7.5	$\mu$ Adc	
		10	—	0.5	—	0.0010	0.5	—	15		
		15	—	1.0	—	0.0015	1.0	—	30		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0 10 15	$I_T = (1.2 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (2.4 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (3.6 \mu\text{A/kHz}) f + I_{DD}$							$\mu$ Adc	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.004$ .

**SWITCHING CHARACTERISTICS\*\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic		Figure	Symbol	$V_{DD}$	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	NAND, NOR	2, 3	$t_{TLH}$	5.0 10 15	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	NAND, NOR	2, 3	$t_{THL}$	5.0 10 15	100 50 40	200 100 80	ns
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 17 \text{ ns}$	NOR-Inverter	3	$t_{TLH}$	5.0 10 15	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (0.67 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{THL} = (0.45 \text{ ns/pF}) C_L + 17.5 \text{ ns}$ $t_{THL} = (0.37 \text{ ns/pF}) C_L + 11.5 \text{ ns}$	NOR-Inverter	3	$t_{THL}$	5.0 10 15	60 40 30	120 80 60	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 45 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 37 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$	NAND	2	$t_{PLH},$ $t_{PHL}$	5.0 10 15	130 70 50	260 140 100	ns
	NOR	3	$t_{PLH}$ $t_{PHL}$	5.0 10 15	115 65 45	230 130 90	ns
	NOR-Inverter	3	$t_{PLH},$ $t_{PHL}$	5.0 10 15	130 70 50	260 140 100	ns

\* The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.**

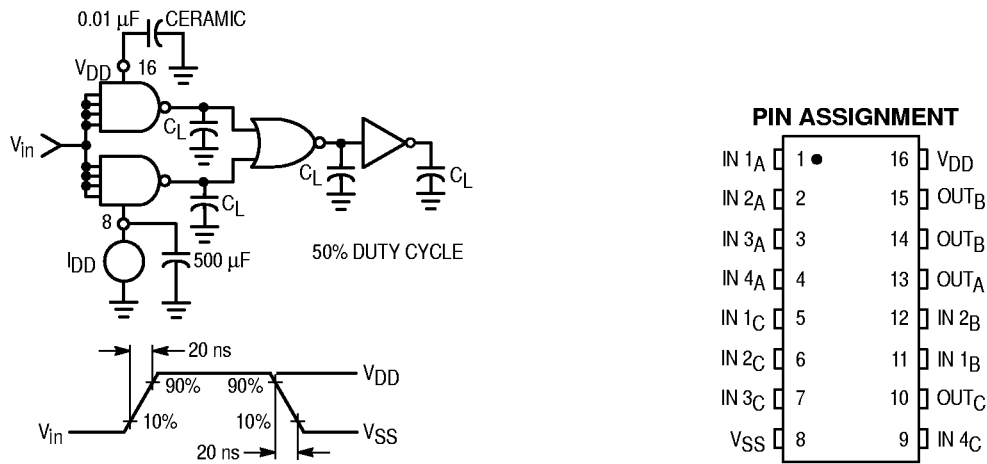


Figure 1. Power Dissipation Test Circuit and Waveform

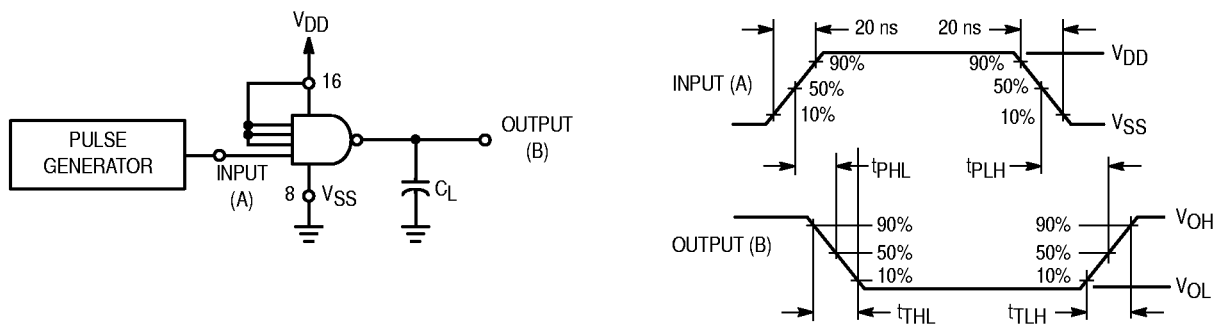


Figure 2. Input "NAND" Gate Switching Time Test Circuit and Waveforms

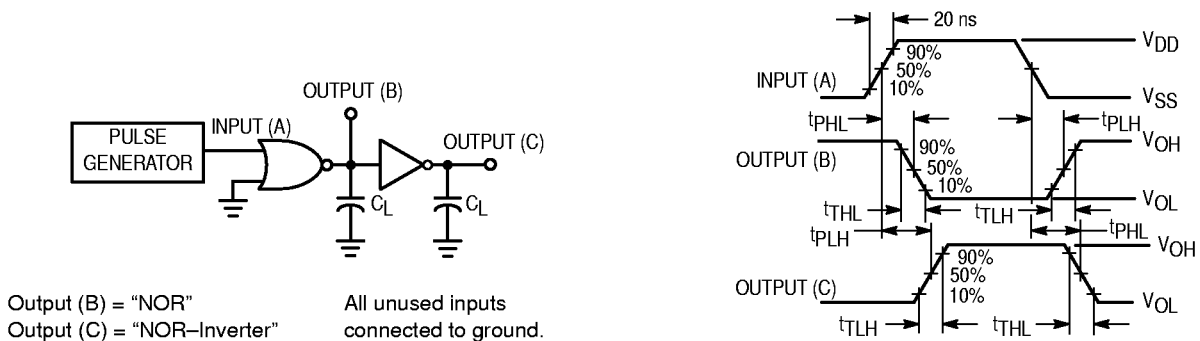
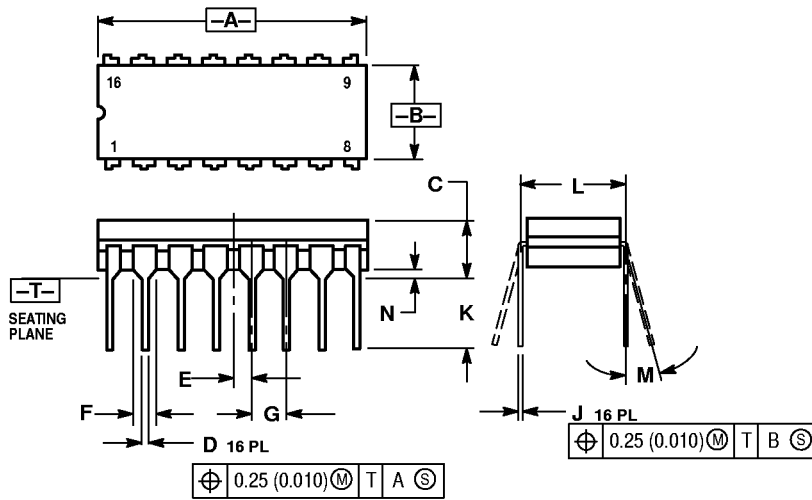


Figure 3. "NOR" Gate and "NOR-Inverter" Switching Time Test Circuit and Waveforms

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

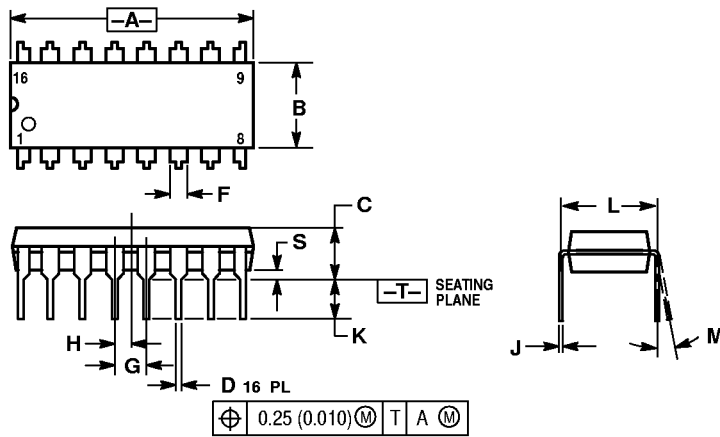


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



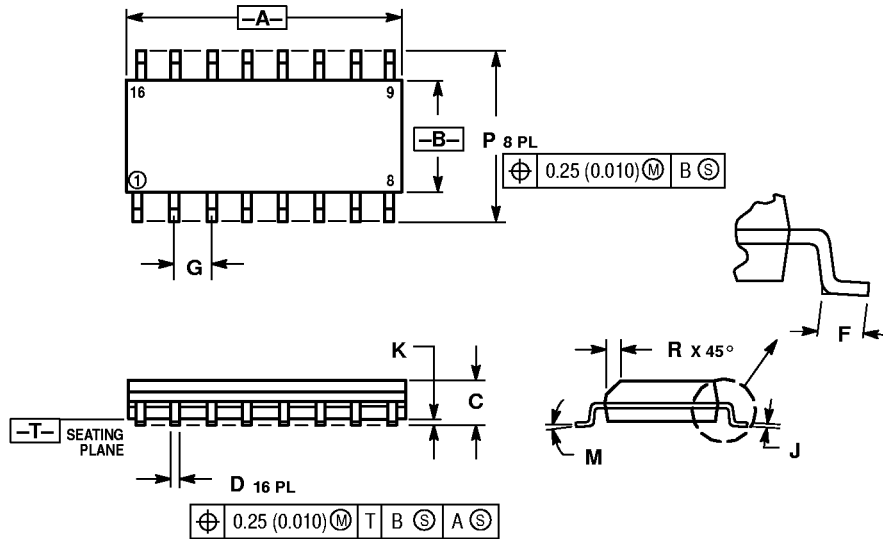
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MC14501UB/D

