Am25S07/Am25S08

Hex/Quad Parallel D Registers with Register Enable

DISTINCTIVE CHARACTERISTICS

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops

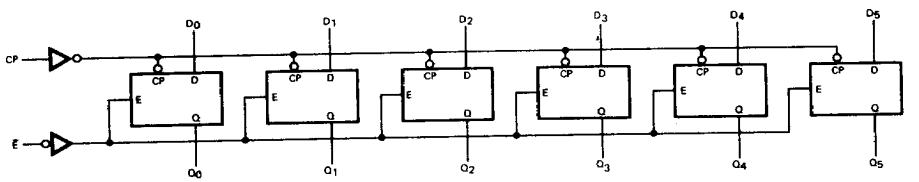
GENERAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

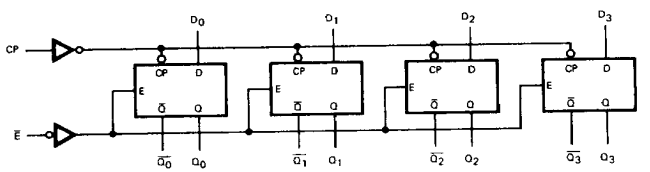
BLOCK DIAGRAM

Am25S07



BD001450

Am25S08



BD001520

RELATED PRODUCTS

Part No.	Description
Am25LS07/08	Low Power Versions
Am2918	Quad D Register
Am2919	Quad Register
Am29821 – 26	8, 9, 10-Bit Register

03702B

Refer to Page 13-1 for Essential Information on Military Devices

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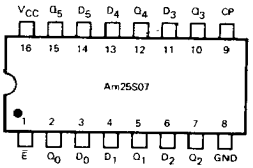
CONNECTION DIAGRAM
Top View

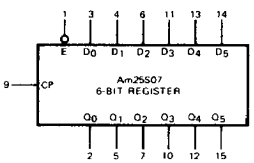
Am25S07



CD001680

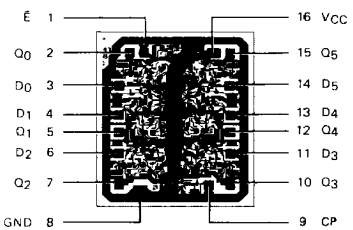
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
Am25S07



LS000590

METALLIZATION AND PAD LAYOUT
Am25S07



DIE SIZE: 0.070" x 0.083"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S07/08 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25S07/08** — Device type
  - Hex/Quad D Registers

Valid Combinations	
Am25S07/08	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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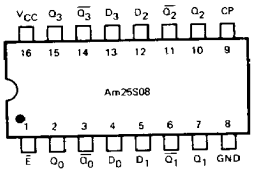
CONNECTION DIAGRAM
Top View

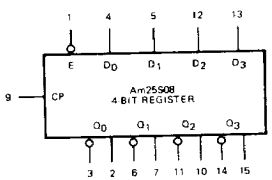
Am25S08



CD001690

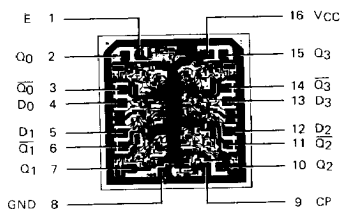
Note: Pin 1 is marked for orientation

LOGIC SYMBOL
Am25S08



LS000600

METALLIZATION AND PAD LAYOUT
Am25S08



DIE SIZE: 0.067" x 0.073"

9

03702B

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D_i	I	The D flip-flop data inputs.
1	$\overline{E}$	I	Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.
9	CP	I	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
	Q_i	O	The TRUE register outputs.
	$\overline{Q}_i$	O	The complement register outputs.

FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_I	CP	Q_I	$\overline{Q}_I$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

H = HIGH
L = LOW
X = Don't Care

↑ = LOW-to-HIGH Transition
NC = No Change
$\overline{Q}_i$ on Am25S08 Only

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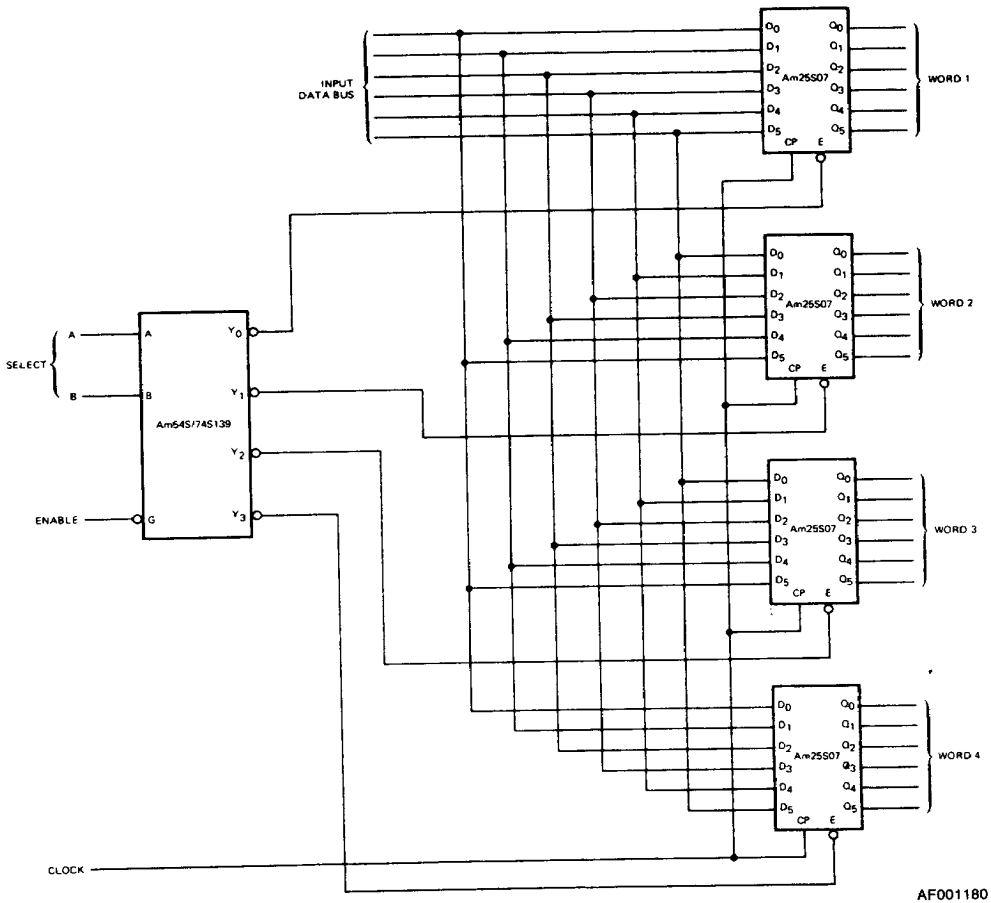
APPLICATIONS



Selective Register Loading of Data on Synchronous Clock.

03702B

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature (Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 16 to Pin 8) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XC	2.7	3.4		Volts
			XM	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	S07		90	144	mA
			S08		60	96	

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

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SWITCHING CHARACTERISTICS (T_A = +25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data		5.5			ns
t_s	Enable		9			ns
t_h	Data		3			ns
t_h	Enable		3			ns

Am25S07 LOADING RULES (In STTL Unit Loads)

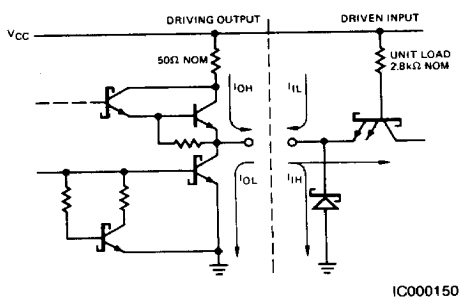
Input/Output	Pin Nos.	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Am25S08 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin Nos.	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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