National Semiconductor

DM74LS952
Dual Rank 8-Bit TRI-STATE® Shift Registers

General Description

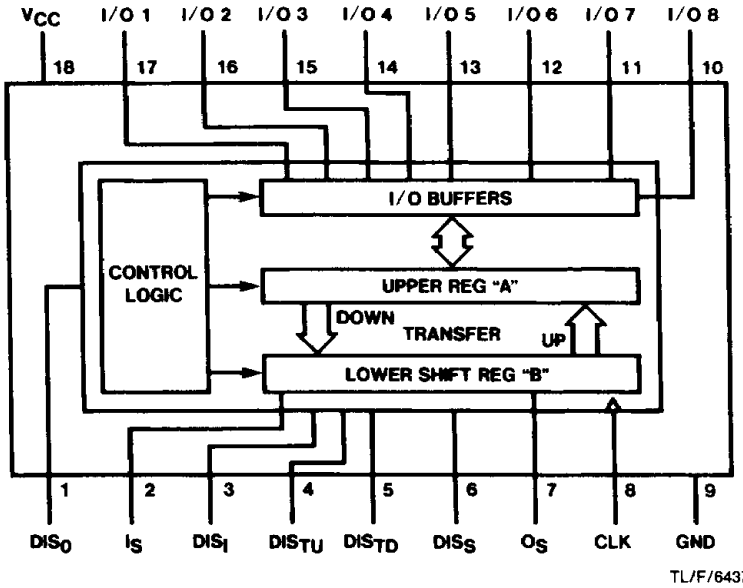
These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", synchronously clear. Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74LS952N
See NS Package Number N18A

Pin Description

DIS_O—Output disable
I_S—Serial input
DIS_I—Input disable
DIS_{TU}—Transfer up disable
DIS_{TD}—Transfer down disable
DIS_S—Shift disable
O_S—Serial output
CLK—Clock
GND—Ground
I/O 1 . . . I/O 8—8-bit I/O pins
V_{CC}—Supply Voltage

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS952			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.8	V
I_{OH}	High-Level Output Current			−5.2	mA
I_{OL}	Low-Level Output Current			16	mA
f_{CLOCK}	Clock Frequency (Note 5)	0		25	MHz
Clock Pulse	High Pulse Width (Note 5)	25	17		ns
	Low Pulse Width (Note 5)	15	7		ns
t_{SET-UP}	Data Set-Up Time (Note 5)	10			ns
t_{HOLD}	Data Hold Time (Note 5)	0			ns
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)		DM74LS952			Units
				Min	Typ (2)	Max	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OH} = −5.2 mA	2.4			V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OL} = 8 mA		0.25	0.4	V
			I_{OL} = 16 mA		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V				−50	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max (3)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (4)			61	99	mA
I_{OFF}	TRI-STATE I/O Current	V_{CC} = Max, V_{IH} = 2V	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

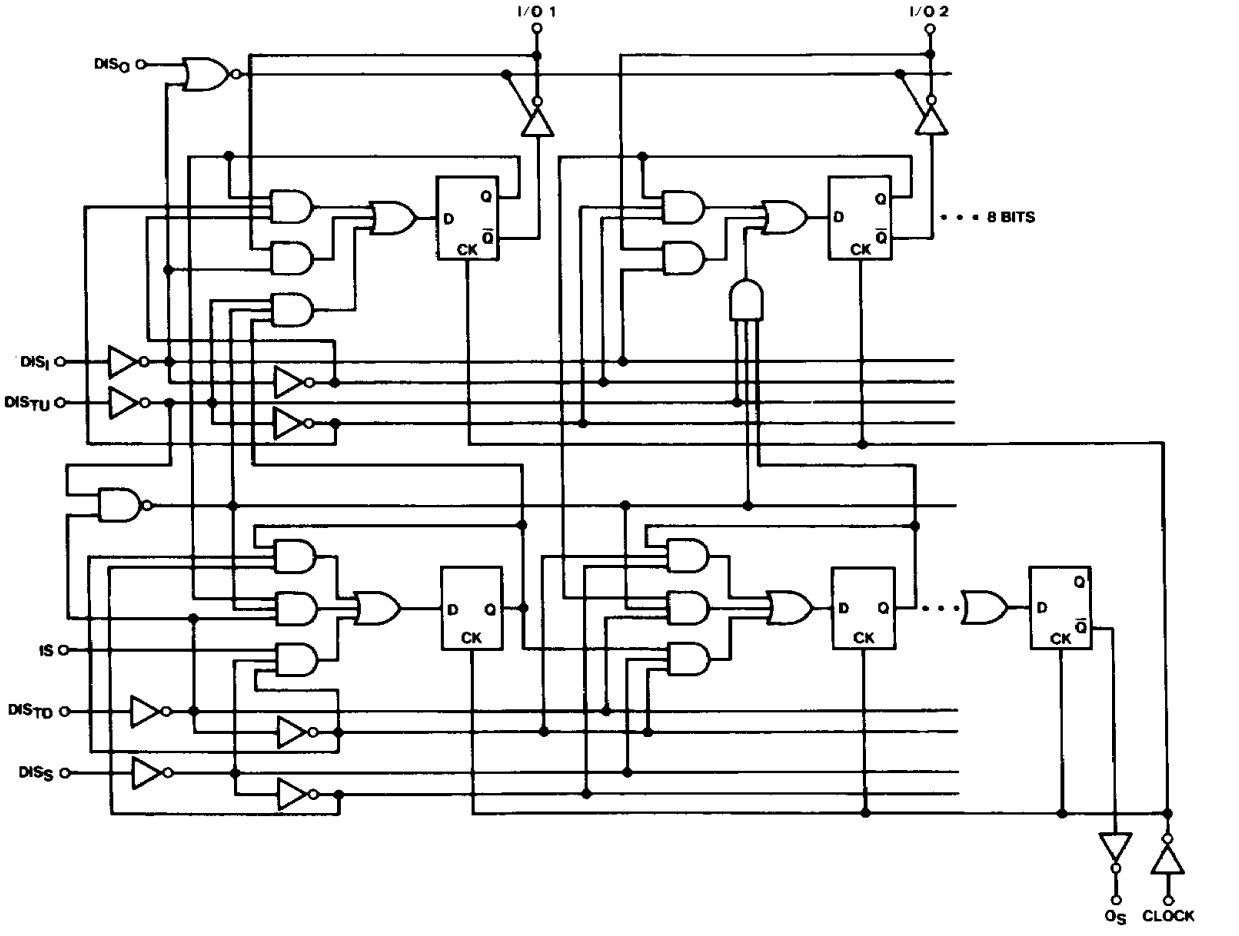
Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4V. All other control inputs and I/O pins grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 1 kΩ	25		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		7	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Output		10	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	24	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	27	ns
t_{PZH}	Output Enable Time to High Level		5	23	ns
t_{PZL}	Output Enable to Low Level		4	18	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 1 kΩ	5	23	ns
t_{PLZ}	Output Disable Time from Low Level		6	27	ns

Logic Diagram



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Function Table

Table I

DIS_O	DIS_I	DIS_{TU}	DIS_{TD}	DIS_S	CLK	I_S	8-Bit I/O Pins	Content of Upper Reg. "A"								Content of Lower Serial Shift Reg. "B"								O_S	Comments
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Entering data from I/O to reg. "A"
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A"
L	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	←	←	←	DOR	→	→	→		b1	b2	b3	b4	b5	b6	b7	b8	b8	Reg. "A" will OR data from I/O to reg. "B"
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B"
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Entering data and transfer down
H	H	L	L	X	↑	X	Hi-Z	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(1) Synchronously clear both registers to
L	H	L	L	X	↑	X	Output	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(2) logic "L" level
X	L	L	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	L	L	L	L	L	L	L	L	L	(3) Enter data to reg. "A" clear reg. "B"
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B"
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	d	b1	b2	b3	b4	b5	b6	b7	b7	Entering data and serial shifting
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	H	L	↑	d	Input	←	←	←	DOR	→	→	→		d	b1	b2	b3	b4	b5	b6	b7	b7	DOR function and serial shifting

X ≡ Don't Care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

a1 . . . a8/b1 . . . b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

I_1 . . . I_8 ≡ The level of steady state inputs of the I/O pins

DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., I_1 + b1, I_2 + b2, I_3 + b3 . . . I_8 + b8

d ≡ Data of the serial input

Timing Diagram

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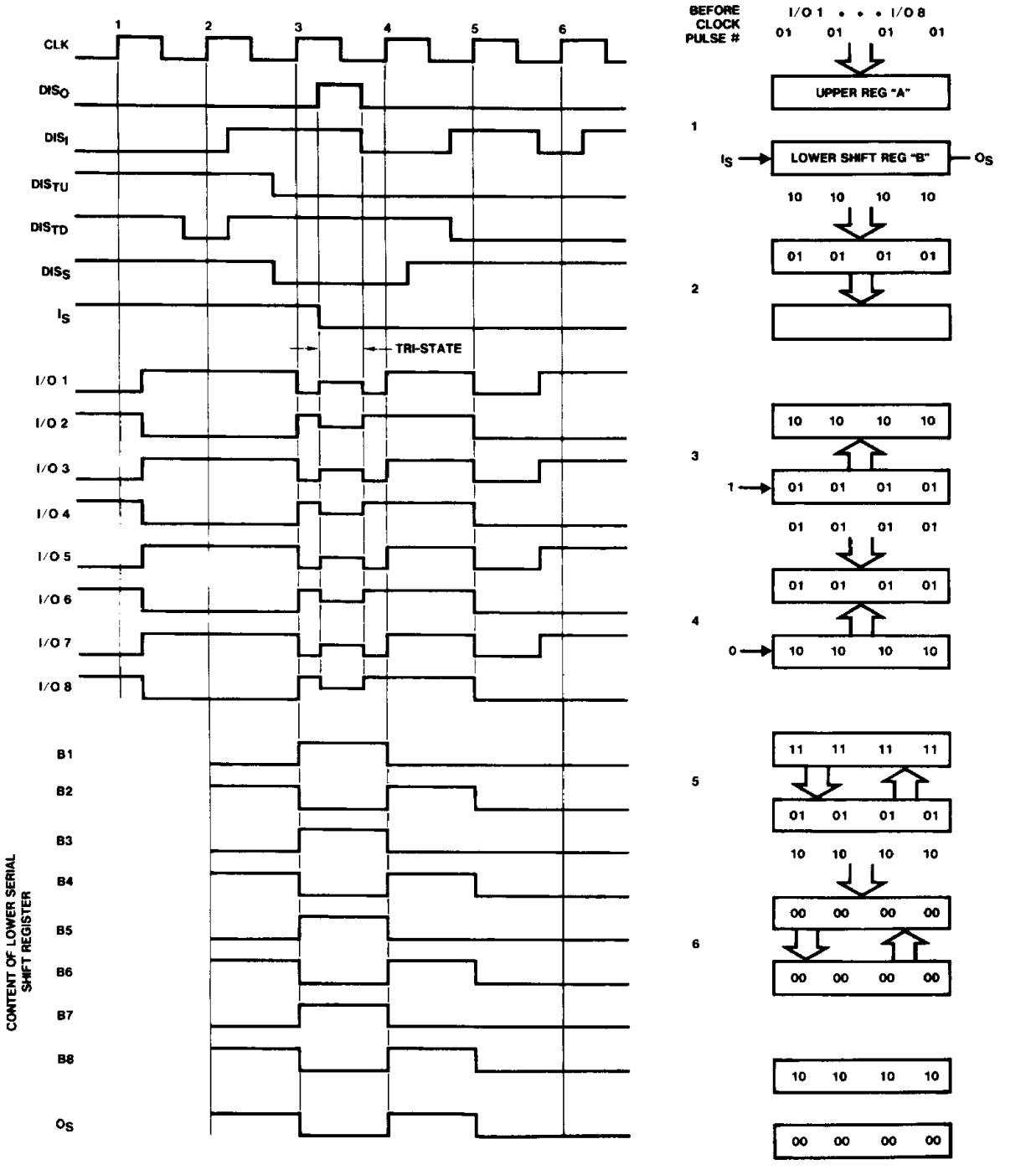

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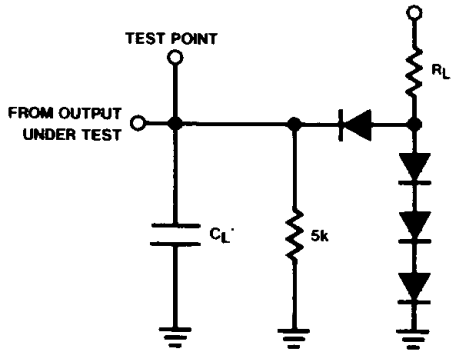
AC Test Circuit and Switching Time Waveforms



All diodes are 1N916 or 1N3064.
C_L includes probe and jig capacitance.

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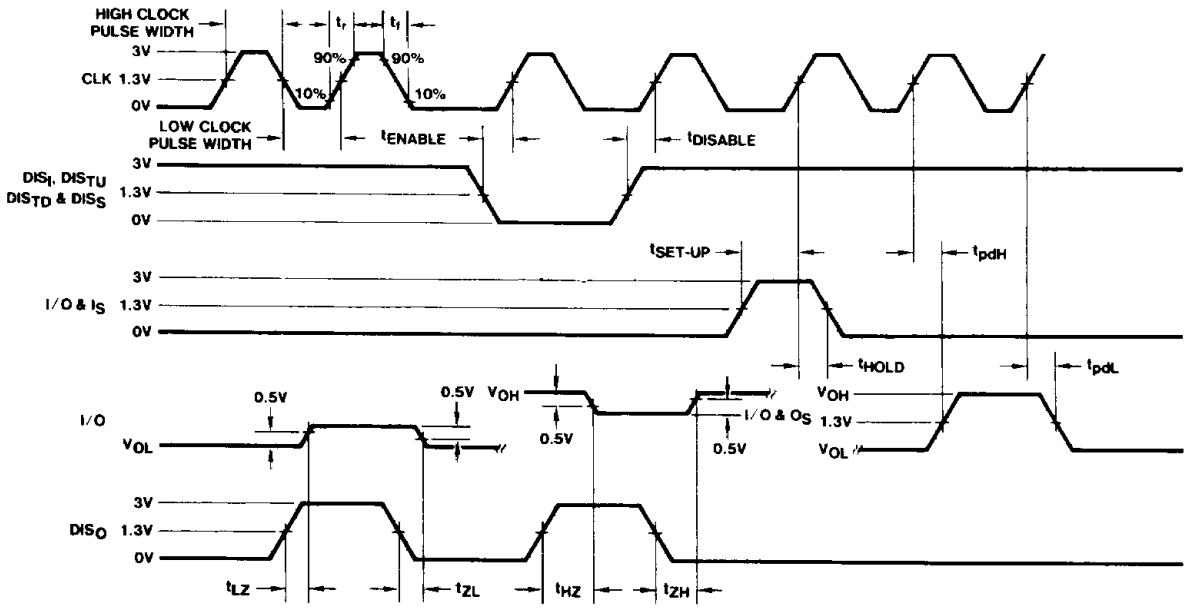

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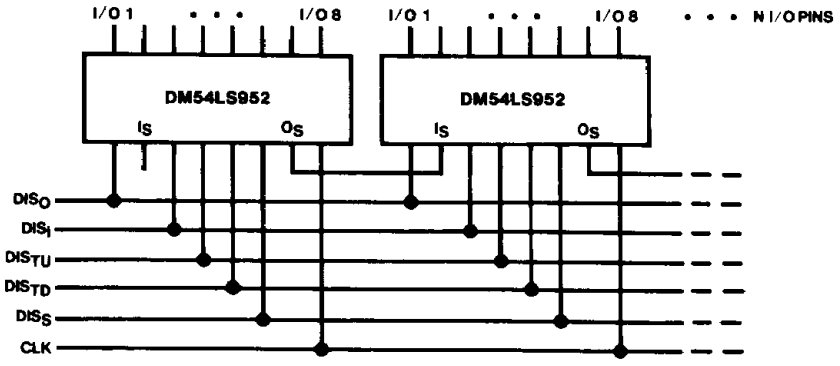
All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, $Z_{OUT} \approx 50\Omega$.

Cascading Packages

Cascading Packages for N-Bit Word



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