

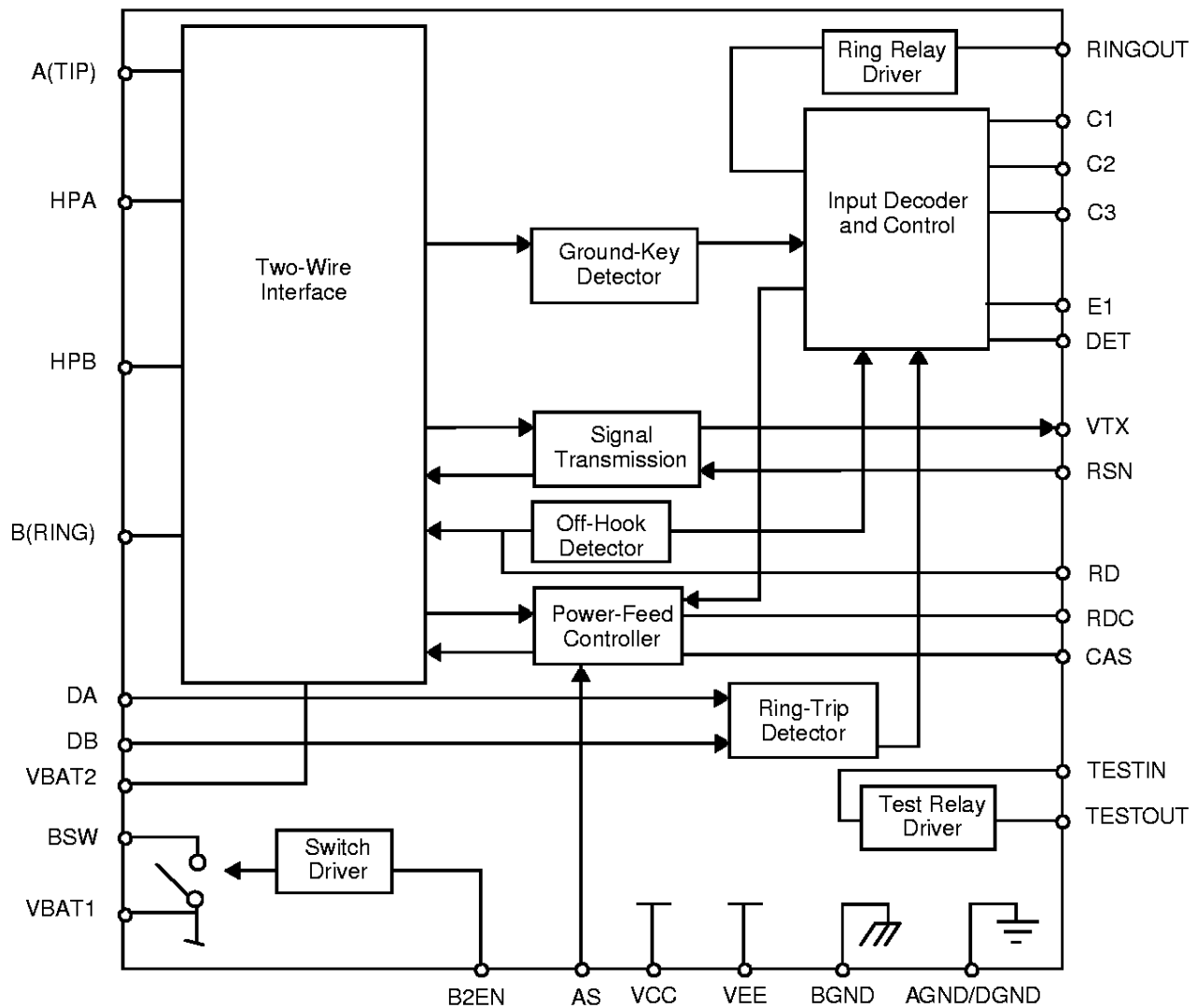
Am7949

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Ideal for Fiber-In-The-Loop (FITL) applications
- Low standby power
- -21 V to -58 V battery operation
- On-chip battery switching and feed selection
- On-hook transmission
- Two-wire impedance set by single external impedance
- Programmable constant-current feed
- Current gain = 200
- Programmable loop-detect threshold
- Ground-key detector
- Tip Open state for ground-start lines
- Polarity reversal option
- On-chip ring relay driver and relay snubber circuit

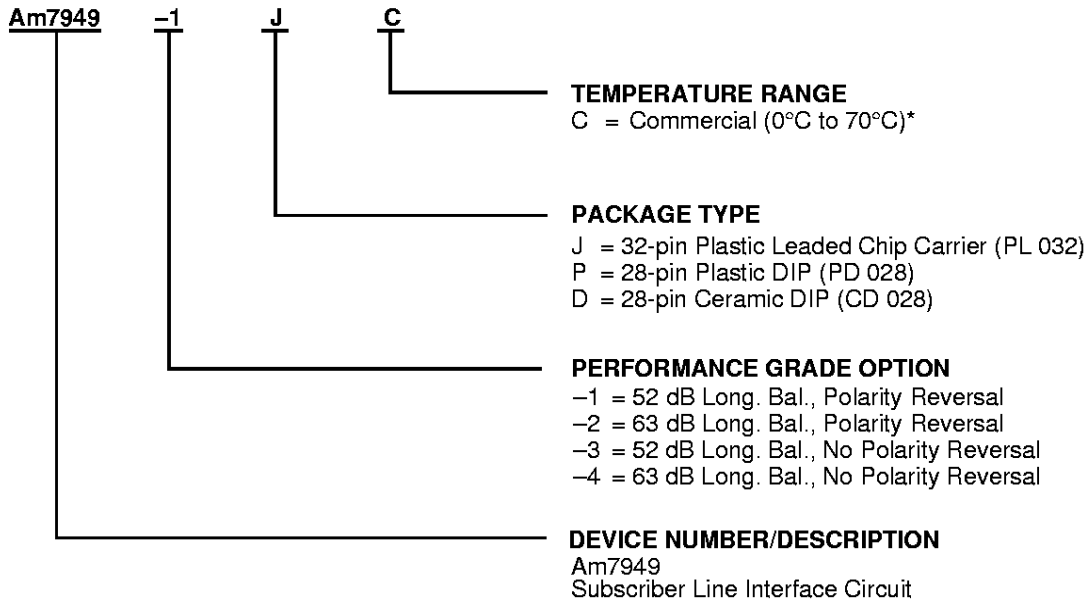
BLOCK DIAGRAM



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am7949	-1	JC
	-2	PC
	-3	DC
	-4	

Valid Combinations

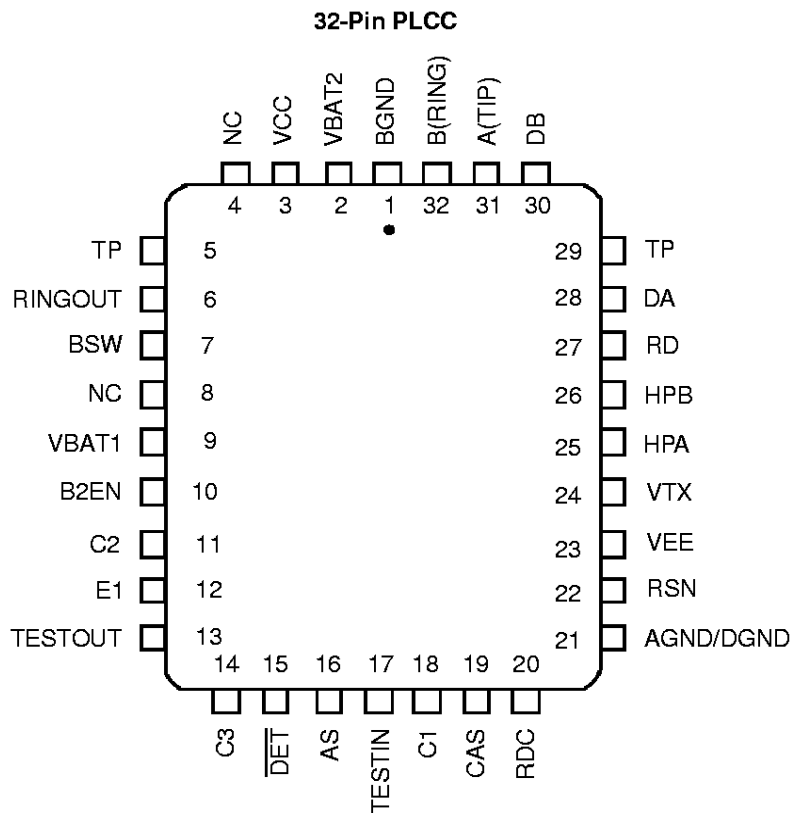
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note:

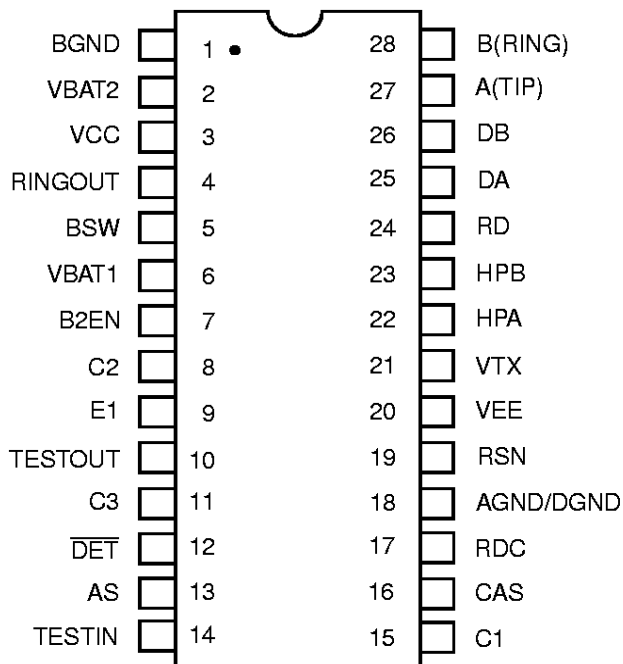
* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

CONNECTION DIAGRAMS

Top View



28-Pin Plastic or Ceramic DIP



Notes:

1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate.
3. NC = No Connect

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
AS	Input	Anti-saturation state select. Logic Low enables battery independent feed. Logic High enables battery tracking anti-sat. TTL compatible.
A(TIP)	Output	Output of A(TIP) power amplifier.
B2EN	Input	VBAT2 Enable. Logic Low enables low power operation from VBAT2. Logic High enables operation from VBAT1. TTL compatible.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
BSW	Battery Switch	Collector of battery switch.
C3–C1	Inputs	Decoder. SLIC control pins. C3 is MSB and C1 is LSB. TTL compatible.
CAS	Capacitor	Anti-saturation capacitor; Pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-Trip Negative; Negative input to ring-trip comparator.
DB	Input	Ring-Trip Positive; Positive input to ring-trip comparator.
DET	Output	Switchhook Detector; A logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C3–C1, E1). The output is open-collector with a built-in 15 k Ω pull-up resistor.
E1	Input	Ground-key enable. A logic High selects the off-hook detector. A logic Low selects the ground key. TTL compatible.
HPA	Capacitor	High-pass filter capacitor; A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor; B(RING) side of high-pass filter capacitor.
NC	—	Pin not internally connected.
RD	Resistor	Detect resistor; Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). The sign of V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver; open-collector driver, emitter internally connected to BGND.
RSN	Input	Receive summing node; The metallic current (both AC and DC) between A(TIP) and B(RING) = 200 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
TESTIN	Input	Test relay driver input.
TESTOUT	Output	Open collector driver with emitter internally connected to AGND.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT1	Battery	Battery supply and connection to substrate.
VBAT2	Battery	Power supply to output amplifiers. Connect externally to BSW. Connect to off-hook battery through a diode.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VTX	Output	Transmit Audio; Unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +150°C
V _{CC} with respect to AGND/DGND	–0.4 V to +7.0 V
V _{EE} with respect to AGND/DGND	+0.4 V to –7.0 V
V _{BAT2} with respect to V _{BAT1}	V _{BAT1} to GND
V _{BAT1} with respect to AGND/DGND:	
Continuous	+0.4 V to –70 V
10 ms	+0.4 V to –75 V
BGND with respect to AGND/DGND	+3 V to –3 V
A(TIP) or B(RING) to BGND:	
Continuous	–70 V to +1 V
10 ms (f = 0.1 Hz)	–70 V to +5 V
1 μs (f = 0.1 Hz)	–80 V to +8 V
250 ns (f = 0.1 Hz)	–90 V to +12 V
Current from A(TIP) or B(RING)	±150 mA
RINGOUT current	50 mA
RINGOUT voltage	BGND to +7 V
RINGOUT transient	BGND to +10 V
DA and DB inputs	
Voltage on ring-trip inputs	V _{BAT} to 0 V
Current into ring-trip inputs	±10 mA
C3–C1, E1, AS, B2EN	
Input voltage	–0.4 V to V _{CC} + 0.4 V
Maximum power dissipation, continuous, T _A = 85°C, No heat sink (See note):	
In 32-pin PLCC package	1.4 W
In 28-pin ceramic DIP package	2.07 W
In 28-pin plastic DIP package	1.13 W
Thermal Data	θ _{JA}
In 32-pin PLCC package	43°C/W typ
In 28-pin ceramic DIP package	30°C/W typ
In 28-pin plastic DIP package	53°C/W typ

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES**Commercial (C) Devices**

Ambient temperature	0°C to +70°C*
V _{CC}	4.75 V to 5.25 V
V _{EE}	–4.75 V to –5.25 V
V _{BAT1}	–40.5 V to –58 V
V _{BAT2}	–21 V to V _{BAT1}
AGND/DGND	0 V
BGND with respect to AGND/DGND	–100 mV to +100 mV
Load resistance on VTX to ground	10 kΩ min

Operating Ranges define those limits between which device functionality is guaranteed.

* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note	
Transmission Performance							
2-wire return loss	200 Hz to 3.4 kHz (Test Circuit D)	26			dB	1, 4, 7	
Z _{VTX} , Analog output impedance			3	20	Ω	4	
V _{VTX} , Analog output offset voltage	0°C to +70°C -40°C to +85°C	-35 -40		+35 +40	mV	— 4	
Z _{RSN} , Analog input impedance			1	20	Ω	4	
Overload level, 2-wire and 4-wire	Active state	2.5			V _{pk}	2a	
Overload level	On-hook, R _L = 600 Ω	0.88			V _{rms}	2b	
THD (Total Harmonic Distortion)	+3 dBm, BAT2 = -24 V		-64	-50	dB	— 5	
THD, on-hook	0 dBm, R _L = 600 Ω, BAT1 = -57.5 V			-35.5			
Longitudinal Performance (See Test Circuit D)							
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz normal polarity normal polarity reverse polarity	-1, -3*	52		dB	—	
		0°C to +70°C -2, -4	63			—	
		-40°C to +85°C -2, -4	58			4	
	1 kHz to 3.4 kHz normal polarity normal polarity reverse polarity	-1, -3*	52			—	
		0°C to +70°C -2, -4	58			—	
		-40°C to +85°C -2, -4	54			4	
Longitudinal signal generation 4-L	200 Hz to 800 Hz normal polarity	42					
Longitudinal current per pin (A or B)	Active or OHT state	12	18		mArms		
Longitudinal impedance at A or B	0 to 100 Hz			35	Ω/pin		
Idle Channel Noise							
C-message weighted noise	R _L = 300 Ω DC	0°C to +70°C		+7	+10	dB _{BrnC}	— 4
	R _L = 300 Ω DC	-40°C to +85°C			+12		
Psophometric weighted noise	R _L = 300 Ω DC	0°C to +70°C		-83	-80	dB _{Bmp}	— 4
	R _L = 300 Ω DC	-40°C to +85°C			-78		
Insertion Loss and Balance Return Signal (2- to 4-Wire, 4- to 2-Wire, and 4- to 4-Wire, See Test Circuits A and B)							
Gain accuracy over temperature	0 dBm, 1 kHz	0°C to +70°C	-0.15	0	+0.15	dB	—
		-40°C to +85°C	-0.20	0	+0.20		4
Gain accuracy over frequency	300 to 3400 Hz relative to 1 kHz	0°C to +70°C	-0.10		+0.10		—
		-40°C to +85°C	-0.15		+0.15		4
Gain tracking	+3 dBm to -55 dBm relative to 0 dBm	0°C to +70°C	-0.10		+0.10		—
		-40°C to +85°C	-0.15		+0.15		4
Gain accuracy, OHT state		-0.5		+0.5		4	
Group delay	0 dBm, 1 kHz			3	μs	1, 4, 7	

Note:

*P.G. = Performance Grade

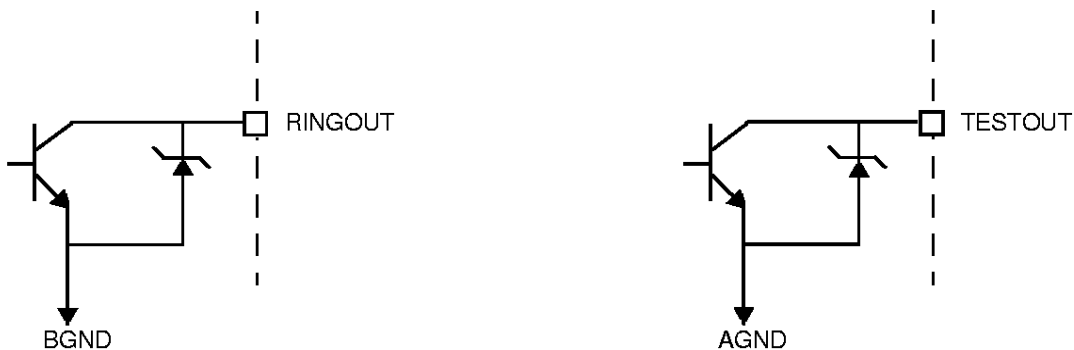
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L , Loop current accuracy	I_L in constant-current region	$0.915I_L$	I_L	$1.085I_L$	mA	
I_L , Long loops, Active or OHT state	$R_{LDC} = 600 \Omega$	20	21.7			
I_L , Accuracy, Standby state	$I_L = \frac{ V_{BAT} - 3 \text{ V}}{R_L + 1800} \quad T_A = 25^\circ\text{C}$	$0.7I_L$	I_L	$1.3I_L$		
	$R_L = 600 \Omega$	15	17.4			
$I_{L\text{LIM}}$	Active, A and B to GND OHT, A and B to GND		50 50	80		4
I_L , Loop current, Open Circuit state	$R_L = 0$			100	μA	
I_A , pin A leakage, Tip Open state	$R_L = 0$			100		
I_B , pin B current, Tip Open state	B to GND B to $V_{BAT1} + 6 \text{ V}$		30 30		mA	
V_A , Active, ground-start signaling	A to $-48 \text{ V} = 7 \text{ k}\Omega$, B to GND = 100Ω	-7.5	-5			4
V_{AB} , Open Circuit voltage	$V_{BAT1} = -51.6 \text{ V}$	42.8			V	
Power Supply Rejection Ratio ($V_{\text{RIPPLE}} = 100 \text{ mVrms}$), Active Normal State						
V_{CC} V_{EE} V_{BAT}	50 Hz to 3400 Hz 50 Hz to 3400 Hz 50 Hz to 3400 Hz	33 29 30	40 35 50		dB	5
Effective internal resistance	CAS pin to GND	85	170	255		
Power Dissipation						
On-hook, Open Circuit state	AS & B2EN = logic high		35	70	mW	
On-hook, Standby state	AS & B2EN = logic high		45	85		
On-hook, OHT state	AS & B2EN = logic high		120	220		
On-hook, Active state	AS & B2EN = logic high		160	230		
Off-hook, Standby state	AS & B2EN = logic low, $R_L = 600 \Omega$		860	1100		
Off-hook, OHT state	AS & B2EN = logic low, $R_L = 300 \Omega$		500	700		
Off-hook, Active state	AS & B2EN = logic low, $R_L = 300 \Omega$		500	700		
Supply Currents, Battery = -58 V						
I_{CC} , On-hook V_{CC} supply current	Open Circuit state		2.0	3.0	mA	
	OHT state		5.3	7.5		
	Standby state		2.3	3.5		
	Active state, $BAT1 = -50 \text{ V}$		5.5	8.0		
I_{EE} , On-hook V_{EE} supply current	Open Circuit state		0.82	2.0		
	OHT state		2.0	3.5		
	Standby state		1.1	2.0		
	Active state, $BAT1 = -50 \text{ V}$		2.0	4.0		
I_{BAT} , On-hook V_{BAT} supply current	Open Circuit state		0.45	1.0		
	OHT state		2.2	4.0		
	Standby state		0.8	2.0		
	Active state, $BAT1 = -50 \text{ V}$		2.8	4.0		

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
RFI Rejection						
RFI rejection	100 kHz to 30 MHz (See Figure E)			1.0	mVrms	4
Logic Inputs (C3–C1, E1, AS, and B2EN)						
V _{IH} , Input High voltage	C3–C1, E1, AS, B2EN TESTIN, I _{IH} = 300 μA	2.0 4.5			V	
V _{IL} , Input Low voltage				0.8		
I _{IH} , Input High current	C3–C1, AS, B2EN	–75		40	μA	
Input High current	Input E1	–75		45		
I _{IL} , Input Low current	C1, C2, C3, E1, AS B2EN	–400 –600				
Logic Output (DET)						
V _{OL} , Output Low voltage	I _{OUT} = 0.8 mA, 15 kΩ to V _{CC}			0.40	V	
V _{OH} , Output High voltage	I _{OUT} = –0.1 mA, 15 kΩ to V _{CC}	2.4				
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Ground-Key Detector Thresholds						
Ground-key resistive threshold	B to GND	2	5	10	kΩ	
Ground-key current threshold	B to GND		9		mA	
Loop Detector						
I _T , Loop-detect threshold	R _D = 35.4 kΩ, I _T = 375/R _D	9.6	10.6	11.6	mA	
Relay Driver Output (RINGOUT/TESTOUT)						
V _{OL} , On voltage, (RINGOUT)	I _{OL} = 30 mA		+0.25	+0.4	V	
V _{OL} , On voltage, (TESTOUT)	I _{OL} = 30 mA, V _{TESTINmin} = 4.0 V		+0.6	+1.0		
I _{OH} , Off leakage	V _{OH} = +5 V			100	μA	
Zener breakover	I _Z = 100 μA	6	7.2	V	V	
Zener On voltage	I _Z = 30 mA		10			

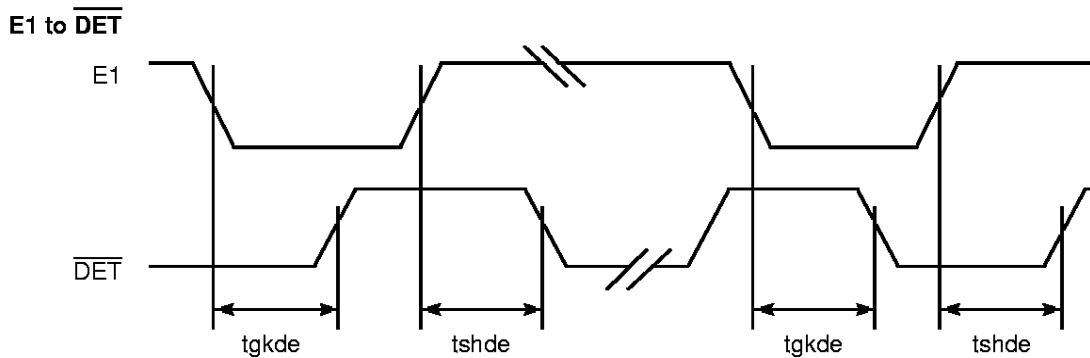
RELAY DRIVER SCHEMATICS



SWITCHING CHARACTERISTICS

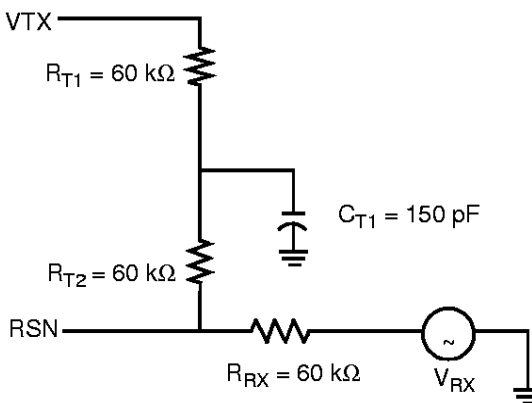
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{\text{DET}}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figure H)	0°C to +70°C			3.8	μs	4
			-40°C to +85°C			4.0		
tshde	E1 Low to $\overline{\text{DET}}$ Low (E0 = 1)	Switchhook Detect state	0°C to +70°C			1.1		
			-40°C to +85°C			1.6		
tshde	E1 High to $\overline{\text{DET}}$ Low (E0 = 1)	Switchhook Detect state	0°C to +70°C			1.2		
			-40°C to +85°C			1.7		
tshde	E1 High to $\overline{\text{DET}}$ High (E0 = 1)	Switchhook Detect state	0°C to +70°C			3.8		
			-40°C to +85°C			4.0		

SWITCHING WAVEFORMS



Notes:

1. Unless otherwise noted, test conditions are $BAT1 = -52\text{ V}$, $BAT2 = -24\text{ V}$, $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$, $R_L = 600\ \Omega$, $R_{DC1} = R_{DC2} = 10\text{ k}\Omega$, $R_D = 35.4\text{ k}\Omega$, no fuse resistors, $C_{HP} = 0.33\ \mu\text{F}$, $C_{DC} = 0.33\ \mu\text{F}$, $C_{CAS} = 0.33\ \mu\text{F}$, $D_1 = 1\text{N400x}$, two-wire AC input impedance is a $600\ \Omega$ resistance synthesized by the programming network shown below.



2. a. Overload level is defined when THD = 1%.
b. Overload level is defined when THD = 1.5%
3. Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
6. Tested with 0 Ω source impedance. 2 M Ω is specified for system design only.
7. Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 μs . The effect of group delay on the linecard performance may also be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.

Table 1. SLIC Decoding

State	C3 C2 C1	2-Wire Status	(DET) Output		Battery Selection
			E1 = 1	E1 = 0	
0	0 0 0	Open Circuit	Ring trip	Ring trip	B2EN
1	0 0 1	Ringing	Ring trip	Ring trip	
2	0 1 0	Active	Loop detector	Ground key	
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key	
4	1 0 0	Tip Open	Loop detector	Ground key	B2EN = 1**
5	1 0 1	Standby	Loop detector	Ground key	V _{BAT1}
6*	1 1 0	Active Polarity Reversal	Loop detector	Ground key	B2EN
7*	1 1 1	OHT Polarity Reversal	Loop detector	Ground key	

Notes:

* Only -1 performance grade devices support polarity reversal.

** For correct ground-start operation using Tip Open, V_{BAT1} on-hook battery must be used.

Table 2. Battery Switching Decoding

AS	B2EN	Operation Status
0	0	Battery independent anti-sat, off-hook battery
1	0	Battery dependent anti-sat, off-hook battery
1	1	Battery dependent anti-sat, on-hook battery

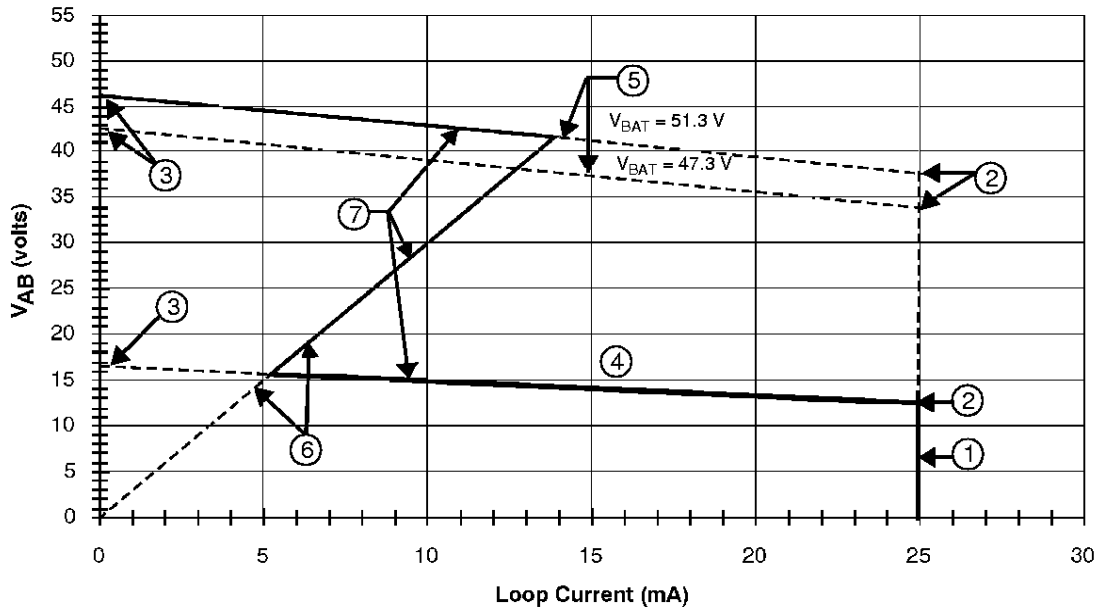
Note:

BSW and V_{BAT2} are connected together externally.

Table 3. User-Programmable Components

$Z_T = 200(Z_{2WIN} - 2R_F)$	<p>Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.</p>
$Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{200 \cdot Z_T}{Z_T + 200(Z_L + 2R_F)}$	<p>Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.</p>
$R_{DC1} + R_{DC2} = \frac{500}{I_{LOOP}}$ $C_{DC} = 1.5 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1} \cdot R_{DC2}}$	<p>R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.</p>
$R_D = \frac{375}{I_T}, \quad C_D = \frac{0.5 \text{ ms}}{R_D}$	<p>R_D and C_D form the network connected from RD to -5 V and I_T is the threshold current between on-hook and off-hook.</p>
$C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi f_c}$	<p>C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.</p>

DC FEED CHARACTERISTICS



$R_{DC} = 20\text{ k}\Omega$

Notes:

1. Constant-current region:

$$I_L = \frac{500}{R_{DC}}$$

2. Anti-sat turn-on point:

$$V_{AB} = 12.5\text{ V, Low-Battery Anti-sat}$$

$$V_{AB} = 1.01|V_{BAT}| - 7.51 - \frac{500}{60}, \text{ High-Battery Anti-sat, } |V_{BAT}| < 50.1\text{ V}$$

$$V_{AB} = 0.338|V_{BAT}| + 26.0 - \frac{500}{60}, \text{ High-Battery Anti-sat, } |V_{BAT}| > 50.1\text{ V}$$

3. Open Circuit voltage:

$$V_{AB} = 16.7\text{ V, Low-Battery Anti-sat}$$

$$V_{AB} = 1.01|V_{BAT}| - 7.51, \text{ High-Battery Anti-sat, } |V_{BAT}| < 50.1\text{ V}$$

$$V_{AB} = 0.338|V_{BAT}| + 26.0, \text{ High-Battery Anti-sat, } |V_{BAT}| > 50.1\text{ V}$$

4. Anti-sat region, Low battery state: $V_{AB} = 16.7 - I_L \frac{R_{DC}}{120}$

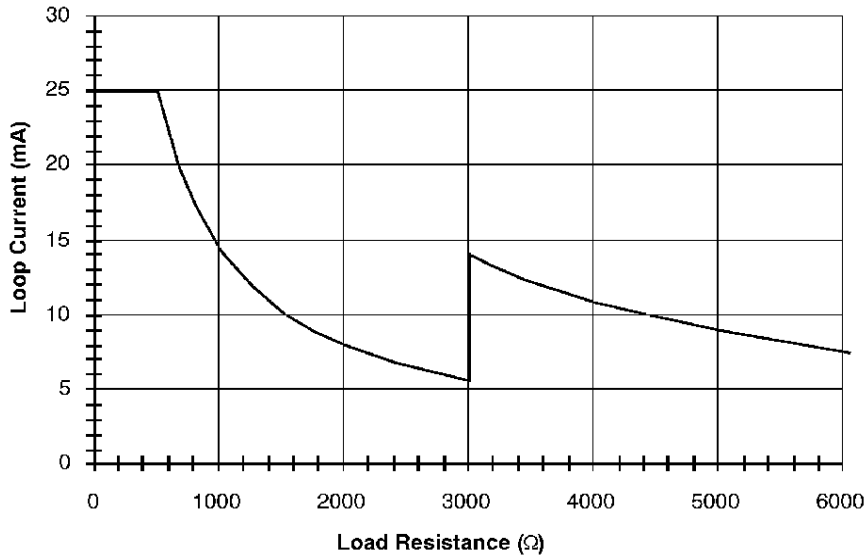
5. Anti-sat region, High battery state: $V_{AB} = 1.01|V_{BAT}| - 7.51 - I_L \frac{R_{DC}}{60}, |V_{BAT}| < 50.1\text{ V}$

$$V_{AB} = 0.338|V_{BAT}| + 26.0 - I_L \frac{R_{DC}}{60}, |V_{BAT}| > 50.1\text{ V}$$

6. Loop resistance at transition between High and Low battery states.

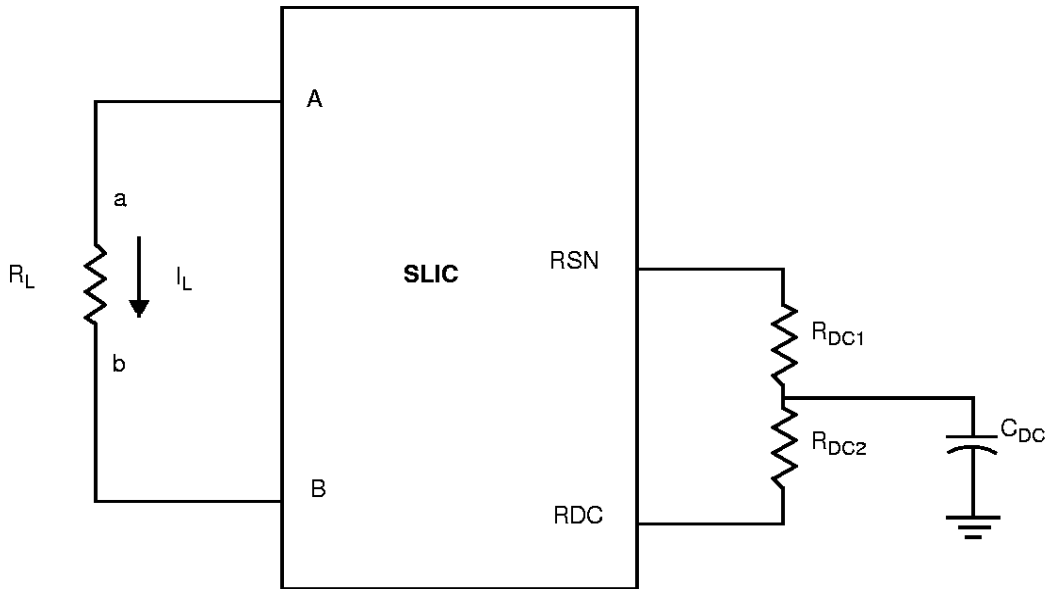
7. DC feed characteristic through High/Low battery transitions, High/Low battery states controlled by on/off-hook states.

a. $V_A - V_B$ (V_{AB}) Voltage vs. Loop Current (Typical)



$R_{DC} = 20\text{ k}\Omega$
 V_{BAT} : High = 51.3 V
 Low = 24 V

b. Loop Current vs. Load Resistance (Typical)

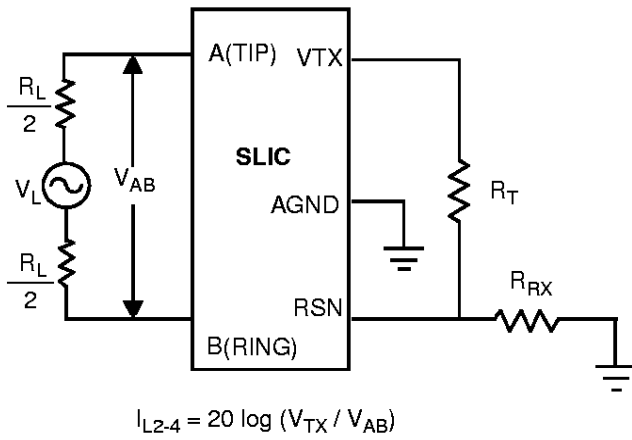


Feed current programmed by R_{DC1} and R_{DC2}

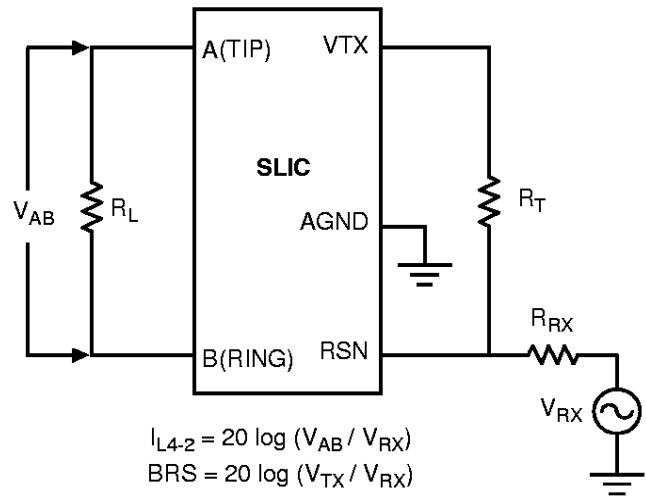
c. Feed Programming

Figure 1. DC Feed Characteristics

TEST CIRCUITS



$$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$$

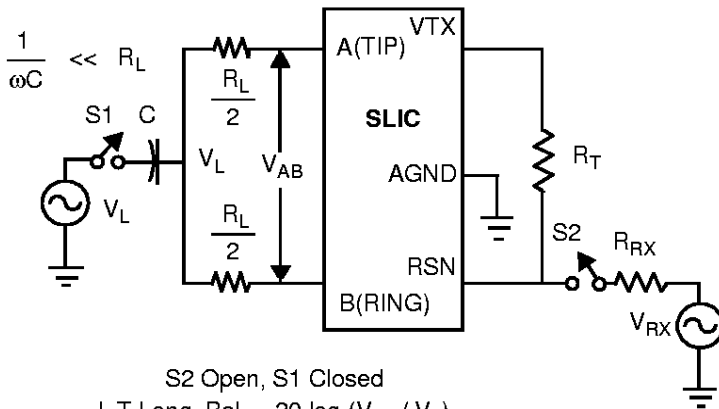


$$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$$

$$BRS = 20 \log (V_{TX} / V_{RX})$$

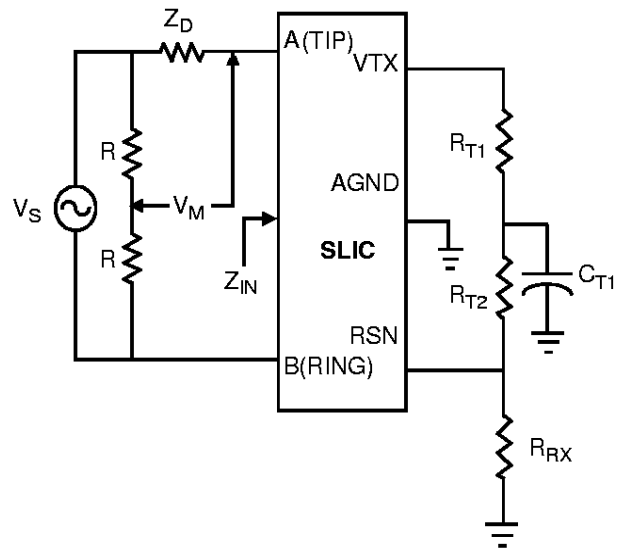
A. Two- to Four-Wire Insertion Loss

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed
 L-T Long. Bal. = $20 \log (V_{AB} / V_L)$
 L-4 Long. Bal. = $20 \log (V_{TX} / V_L)$
 S2 Closed, S1 Open
 4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance

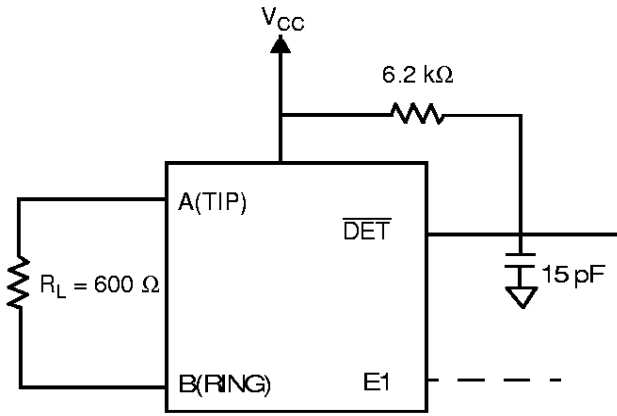


Note:
 Z_D is the desired impedance (e.g., the characteristic impedance of the line).

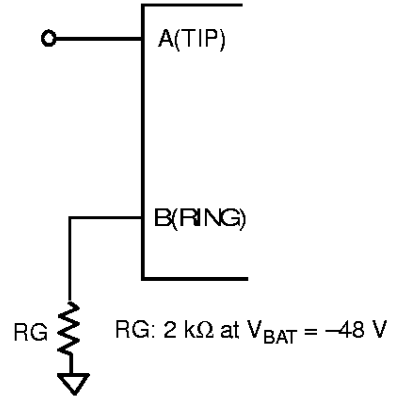
$$R_L = -20 \log (2 V_M / V_S)$$

D. Two-Wire Return Loss Test Circuit

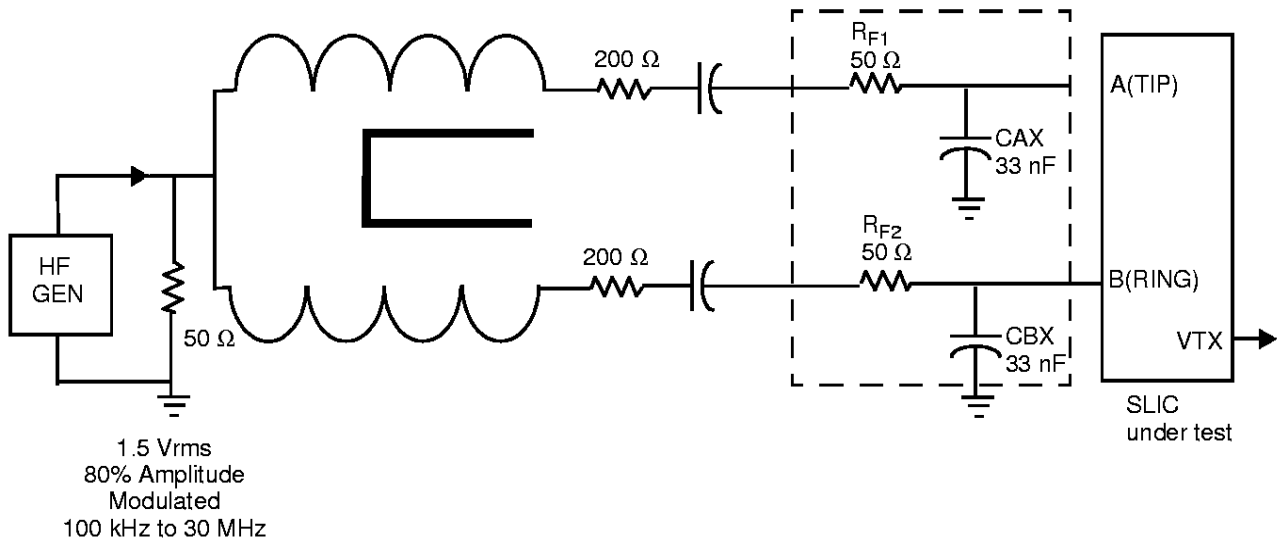
TEST CIRCUITS (continued)



E. Loop-Detector Switching

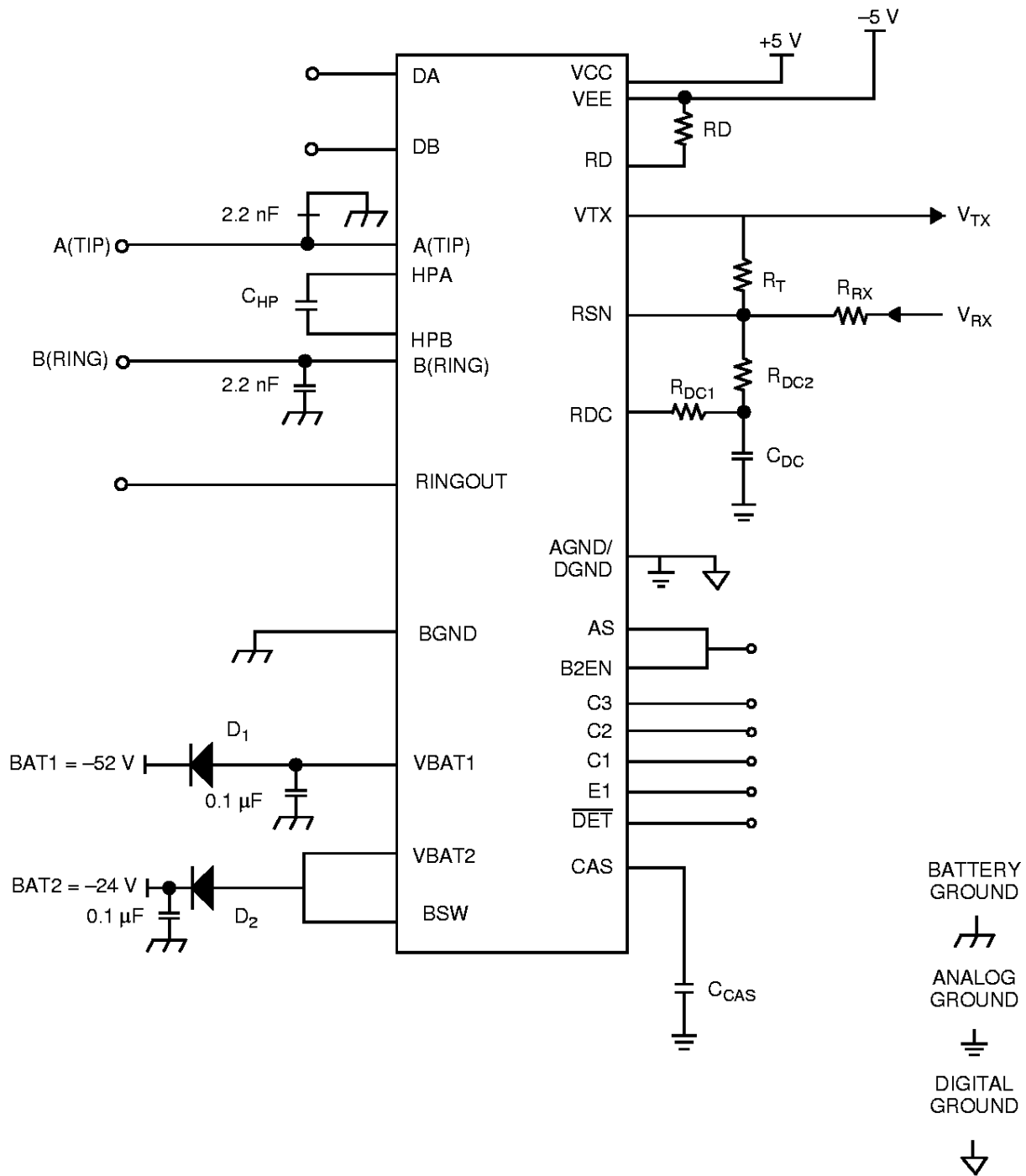


F. Ground-Key Switching



G. RFI Test Circuit

TEST CIRCUITS (continued)



H. Am7949 Test Circuit

REVISION SUMMARY

Revision A to Revision B

- Minor changes were made to the data sheet style and format to conform to AMD standards.
- Electrical Characteristics—Under Longitudinal Performance, the specifications for Longitudinal to Metallic moved from the Typ column to the Min column.
- Electrical Characteristics—Under Line Characteristics (the last row) in the Test Conditions column, $V_{BAT1} = 50\text{ V}$ changed to $V_{BAT1} = 51.6\text{ V}$.
- SLIC Decoding Table—Added B2EN reference to the Battery Selection column and its corresponding note to the notes section.
- DC Feed Characteristics—Added new equations and revised existing ones.

Revision B to Revision C

- Minor changes were made to the data sheet style and format to conform to AMD standards.
- In Pin Description table, inserted/changed TP pin description to: “Thermal pin. Connection for heat dissipation. Internally connected to substrate (VBAT). Leave as open circuit or connected to VBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation.”

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